

IBM

Customer Engineering
Manual of Instruction

7302 Core Storage

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FOREWORD

This manual was prepared for teaching purposes and as an aid for learning the IBM 7302 Magnetic Core Storage unit. Text and illustrations explain basic ferrite core theory, the IBM 7302 core array, logic circuits for actual core storage operations, and special transistor circuits used in the IBM 7302 Magnetic Core Storage Unit. Notations are inserted to make the manual compatible with all computer systems using the 7302 Core Storage Unit.

All material was prepared from information relating to production at a given engineering change level; use of this manual as a reference is subject to future engineering changes.

IBM 7302 CORE STORAGE

THE IBM 7302 Core Storage Unit is a high-speed storage device. Information is stored within the unit as either instructions or data. Instructions are orders, or commands, for the attached computing system to perform some logical operation. Data are information acted upon by instructions.

The storage medium is a small ferrite toroid (magnetic core) which, when magnetized, retains this magnetism. The ability of the core to retain the magnetism allows the core to remember. The core is magnetized by driving current in wires which pass through the core.

Information is stored as words. Each word is composed of 72 cores. Since a core can be magnetized in either of two directions, or states, the information it can contain may be considered as a 0 or a 1. A word, then, consists of 72 ones or zeros in binary form, referred to as bits of information. The word "bit" is derived from binary digit.

Each word in storage is assigned an address, or identifying number, which designates its location in the storage unit. The 16,384 words in the storage unit are designated by the numbers 0; 1; 2... 16,384.

Reading a word from core storage is accomplished by first setting all cores of the addressed word to 0. Any core that was in a one status causes a voltage pulse to appear on the sense winding which passes through all cores. The voltage pulse is amplified and fed into an output register. A regeneration, or rewrite, cycle is then executed. This cycle takes the information from the output register and writes it back into the cores, permitting the information from a particular address to be used on subsequent cycles.

To write a new word into core storage, the cores in the addressed word are set to zero; however, no output is taken from the sense winding. The new word is fed from the core storage input bus to the output (data) register. The rewrite cycle then feeds the information to the cores of the selected address from the output register.

The advantages of core storage over any other storage medium is its ability to read or write at any address with only 1.05 microseconds delay for access time. (Access time is the time required for a word to be read out of storage into the output register).

The IBM 7302 Core Storage Unit is a random-access unit with a word capacity of 16,384 72-bit words. In 7090 systems, the 72-bit word stored in core storage is used as two 36-bit words. As a result, the word capacity is effectively doubled and a total of 32,768 36-bit words may be stored. Cycle time of the unit is 2.0 microseconds and access time is 1.05 microseconds.

The unit is an independent, asynchronous unit that contains the logic to decode the storage address, perform the regeneration cycle, and provide all timing pulses.

The core array is composed of IBM 23 ferrite cores. The logic is composed of current mode transistor circuits, as in the rest of the data processing system.

1.0.00 CORE STORAGE FUNDAMENTALS

1.1.00 FERRITE CORES AS STORAGE DEVICES

A ferrite core is a storage device that can store information in the form of magnetic flux. Information stored in core memory may be either data or instructions.

1.1.01 Physical Properties

A core is a small, flat, doughnut-shaped piece of ferrite material prepared from iron oxides, zinc, manganese, and nickel. These materials are ground to a fine powder, carefully mixed with a binder, and pressed into shape by automatic, high-speed presses. After firing in a kiln, the ferrite core is hard and brittle.

Ferrites have great reliability and low cost. Another desirable property is the high resistivity (10^4 to 10^6 ohms/cm) of the ferrite material which makes eddy current losses and shielding requirements negligible, and results in a faster, more efficient material.

1.1.02 Magnetic Properties

The ferromagnetic properties of the core permit it to be magnetized by applying an external magnetizing action or magnetomotive force (MMF). Wires inserted through the core carry electric current which generates the MMF. After the core is magnetized, it retains the magnetic flux even though the MMF is removed. This property makes the core useful as a storage device.

Under static conditions, the ferrite core is magnetized in one of two possible stable states, hence the term bistable. Items G and K in Figure 1.1-1A show flux lines around a cross section of a ferrite core in each of the two stable states.

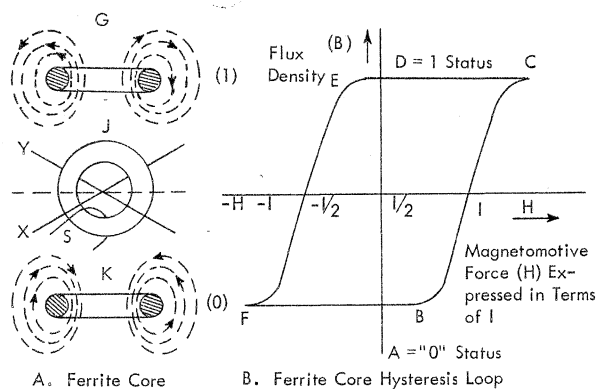


FIGURE 1.1-1. FERRITE CORE CHARACTERISTICS

In Figure 1.1-1B, magnetomotive force, H , is plotted horizontally; flux density, B , is plotted vertically. If a large positive H , represented by the current I , is applied, the core retains a flux density of D after the magnetizing force has returned to zero. Similarly, if a large negative I is applied to the core, the flux follows the path D, E, F . Then the core retains a residual magnetism equivalent to A after the negative I has been removed. Currents greater than I or $-I$ have little effect on the flux density, B , since the core is saturated. Point D , with a flux pattern as shown in G , Figure 1.1-1A, is arbitrarily assigned to stand for a binary 1; point A , with a flux pattern as shown in K , stands for a 0. When current is applied to flip the core from one status to the other, this change is detected by an additional wire called the sense winding (wire S of J in Figure 1.1-1A).

Assume the core is in state D , Figure 1.1-1B, when $-I$ is applied (current to drive the core is supplied through two wires marked X and Y in Figure 1.1-1A); the change in flux as the core goes from state D to state A induces a voltage in the sense winding. A voltage pulse indicates that the core had contained a 1. If the core had been at point A originally, the application of $-I$ would have had little effect on the flux density and induced little voltage in the sense winding. Absence of a voltage pulse indicates that the core contained a 0.

1.2.00 COINCIDENT CURRENT ADDRESSING

For the use of large numbers of ferrite cores to be practical, magnetic material with a nearly square hysteresis curve is essential. Note that magnetic forces resulting from $I/2$ or $-I/2$ have little effect on the flux density, whether or not the core is at state C or D . Switching, or address selection depends on the ability of the core to discriminate between $I/2$ and I .

Impulsing one X and one Y drive line (Figure 1.2-1) is a means of selecting one core from a group. Consider two parallel wires through a ferrite core, each carrying $I/2$ in the same direction. The resulting MMF from each wire is additive and equivalent to the effect of one wire carrying full I current. Now rotate one wire 90 degrees; with the same currents, the combined effect is still additive and still produces sufficient MMF to flip the core. Because the ferrite core must be capable of being set to either a "0" or a "1" status, each X and Y drive line must be capable of driving current in two directions through the plane.

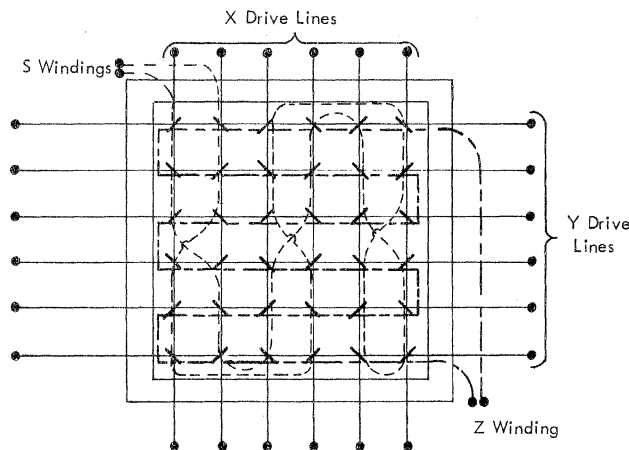


FIGURE 1.2-1. 6 X 6 CORE PLANE

To interrogate any core in Figure 1.2-1, impulse the one applicable X drive line and one Y drive line with $-I/2$. Only one core is affected by the sum of the two currents. If it had contained a 1, a voltage pulse which could be amplified would be induced in the sense winding. If the addressed core had contained a 0, little voltage would be induced in the sense winding. Notice that the state of flux in the other cores along the two drive lines is changed only slightly by the $-I/2$, and they contribute little to the voltage induced in the sense winding. A core with only $-I/2$ flowing through it is called a half-selected core and does not flip.

1.3.00 FERRITE CORE PLANE

Physical arrangement of the cores is shown in Figure 1.2-1. Individual cores are held in place by the four wires which pass through them. The wires are fastened to a frame and the unit is termed a plane. Only one X and one Y line conduct current at any one time. As a result, in the 6 x 6 plane shown, one core is selected and ten cores are half-selected. The sense winding is wound parallel to the X drive lines in a pattern which causes cancellation of half-select noise. This prevents the induction of half-select current which could cause a 1 to read out when the core is actually in a 0 status. Individual cores within the plane are arranged in such a pattern that their magnetic fields are 90° to each other; this eliminates interference between cores. A Z winding (inhibit winding) is wound parallel to the Y drive lines. The inhibit winding carries half-select current. Its function is to cancel the Y drive current through a core and prevent it from flipping (prevent the core from changing from a 0 status to a 1 status). Current flow in the inhibit winding is in such a direction as to oppose Y drive current during a write cycle when data are being fed into the cores.

1.4.00 FERRITE CORE ARRAY

All core storage units require many bits of information to be available. Because only one core in a plane can be addressed during one cycle, there must be a separate plane for each desired bit, i.e., if 36 bits are required, there must be 36 planes and so on. Therefore, the planes are stacked to form an array.

The X and Y lines (Figure 1.4-1) are connected together so X and Y drive current passes through all planes. A core is selected in each plane at the corresponding intersection of X and Y drive lines. Each plane has a separate sense winding and inhibit winding, allowing the sensing and inhibiting of each plane to be done separately.

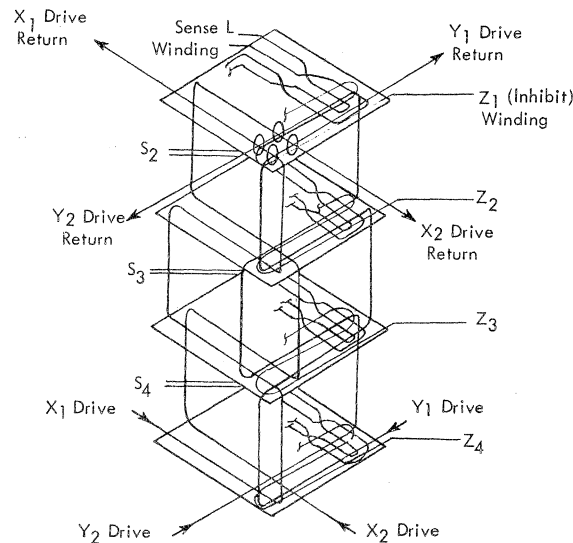


FIGURE 1.4-1. CORE ARRAY WINDINGS

1.5.00 MATRIX SWITCHES

Matrix switches are used to develop the X and Y drive line current in the array. A matrix switch is essentially a pulse transformer; however, its characteristics are similar to those of a bistable ferrite core. It is a load sharing device which combines the power from several sources to form a single, high-powered output pulse.

Each matrix switch has an input (primary winding), which is fed from transistor current drivers, and an output (secondary winding), which goes directly through the array. The way in which the matrix switch cores are wound allows them to be used as an integral part of the address decoding circuits.

1.5.01 Physical Properties

Matrix switch cores are 125 mils inside diameter, 250 mils outside diameter, and 1.8 inches long. The core material is brittle and hard to work, so the core is made in 12 sections. These are arranged in two adjacent stacks of six sections each (Figure 1.5-1A) to reduce winding length. The cores are molded in a heat-conducting plastic in groups of 16 pairs of cores. Groups of 16 were chosen for optimum address circuitry. Each core has a one-turn primary winding, a nine-turn secondary winding, and a one-turn bias winding.

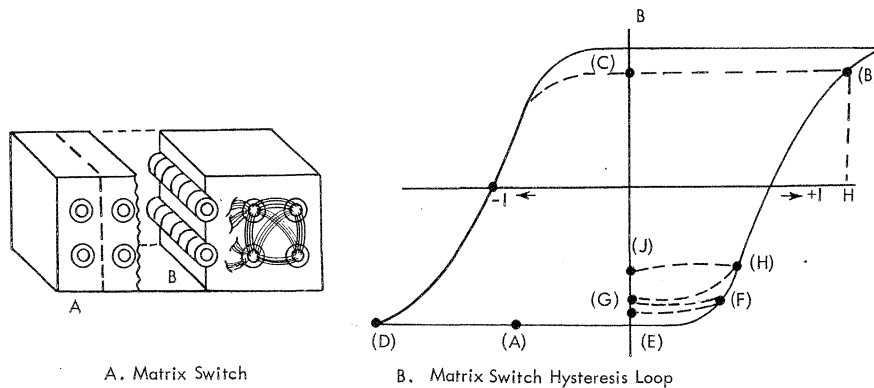


FIGURE 1.5-1. MATRIX SWITCH CHARACTERISTICS

1.5.02 Magnetic Properties

Figure 1.5-1B shows the hysteresis curve for the matrix switch core. Note that the hysteresis loop is nearly square. The core material was chosen for its properties of high flux density and ease of magnetization. A bias winding is used to establish a static operating point (point A) which offers two advantages:

1. Without bias, the static operating point on the hysteresis curve would be at E. Because small fluctuations in primary drive current are unavoidable, the operating point of the core may be driven from E to F; from there, it returns to point G. Subsequent fluctuations drive it from G to H, and back to J. Eventually, when the switch core is selected, the change in flux on driving the core from J to B causes a reduced value of X or Y drive line current, which may fail to flip a selected ferrite core in a plane.
2. Small fluctuations in input current do not drive the matrix switch core beyond the knee of the hysteresis curve. As a result, very little flux change results and the noise induced from matrix switches is negligible.

In system operation, during any core storage cycle, the selected ferrite core is driven in one direction and, a few milli-microseconds later, it is driven in the opposite direction. In Figure 1.5-1B, this drive current is developed by first driving the matrix switch core from point A to point B. A short time later, the switch core is driven from point C to point D, which develops the drive current in the opposite direction.

1.5.03 Matrix Switch Selection and Decoding

By properly wiring a group of matrix switches, only one switch core in the group will produce output current. All input currents are additive in one core, and all other cores experience complete current cancellation. Because several inputs are used to produce one output, relatively low power transistors may be used.

Figure 1.5-2 shows four matrix switch cores. Lines 1, 2, 3, 4, and $\bar{1}, \bar{2}, \bar{3}, \bar{4}$ carry a large enough current that if four of them pass current in the same direction through a core, an output current of $I/2$ flows in the drive line. Current passing through a core in a direction E is assumed to cause an output of $I/2$. Current in a direction F causes an output of $-I/2$. At any one time, current flows in one line of each of the four sets of complement lines; i.e., current flows in either 1 or $\bar{1}$, 2 or $\bar{2}$, and so on. In this manner any one of the four cores may be selected to conduct output current in either the $I/2$ or $-I/2$ direction.

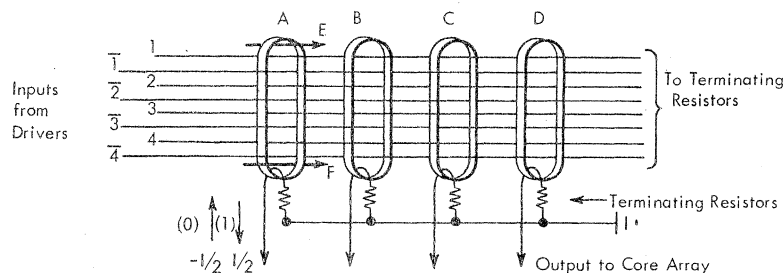


FIGURE 1.5-2. MATRIX SWITCH WIRING

Assume current flow in lines 1, 2, 3, and 4. Note that all wires going through core A are in the same direction. The total current of all four lines causes a large change in flux and, through the transformer action of the core, $I/2$ appears on the output. Core B has no output since lines 1 and 3 pass through it in one direction while lines 2 and 4 pass through it in the opposite direction. These lines cancel each other, as all lines carry equal current. Similar cancellation occurs in cores C and D. By looking at Figure 1.5-2, the combination required for any condition can be determined; i.e., current in lines 1, 2, $\bar{3}$, and $\bar{4}$ causes $I/2$ on the output of core C. For any given set of four lines, cancellation of current occurs in three cores, while an output, or adding of all four lines, occurs in the fourth core.

Note that proper wiring of the matrix switches gives three results:

1. Output current to drive the ferrite cores
2. Address decoding
3. Load sharing properties which allow relatively low power transistors to operate the matrix switch cores.

The matrix switches used in the 7302 core storage are manufactured in groups of 16. Because two inputs are required for each switch core in the group, 32 drive lines are used.

2.0.00 7302 CORE ARRAY

THIS SECTION DEALS specifically with the 79-plane core array used in the IBM 7302 Core Storage Unit (Figure 2.0-1). Planes A through D contain the matrix switch cores. Three blank planes are inserted ahead of the 72 planes of ferrite cores. Three blank planes are inserted ahead of the 72 planes of ferrite cores.

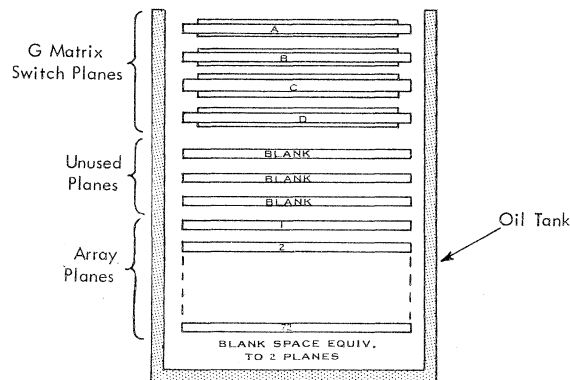


FIGURE 2.0-1. SIDE VIEW OF CORE ARRAY

Attached to the same frame are six gates which contain all the terminating resistors for the X, Y, and Z drive lines (Figure 2.0-2). There are terminating resistors for both the primary and secondary windings of the matrix switches.

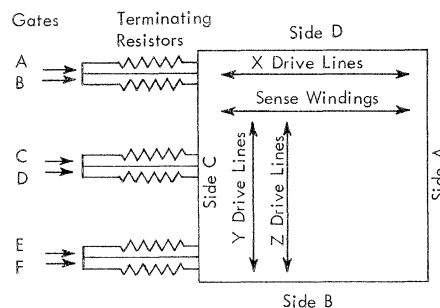


FIGURE 2.0-2. TOP VIEW OF CORE ARRAY

2.1.00 IBM 23 FERRITE CORE PLANE

The IBM 23 ferrite core dimensions are 30 x 50 x 12 mils. Its characteristics are described in Section 1.1.02. To flip the IBM 23 core, 1.17 amps are required. Output on the sense winding is approximately 130 millivolts.

With a large drive current and a small core, heat becomes a problem because the temperature of a core affects its hysteresis loop. As the temperature increases, the loop elongates, and the flux change caused by half-select current can reach objectionable proportions. To maintain a safe temperature throughout the array, the complete unit (terminating resistor gates, core array, and matrix switches) is immersed in an oil-filled tank. By regulating oil temperature a constant tank temperature may be maintained.

2.1.01 Sense Windings

The sense winding is wound to give cancellation of half-select noise (Figure 2.1-1). This winding is segmented into four windings per plane to reduce the delay from core output to sense amplifier. The outputs of the four windings are OR'ed together in the sense amplifier.

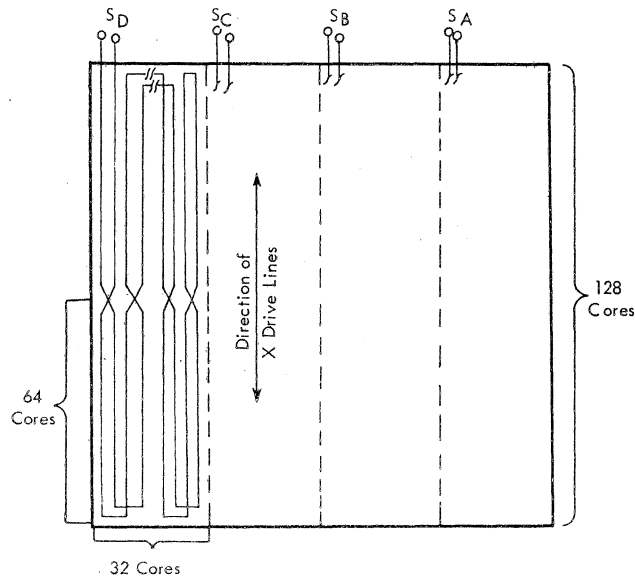


FIGURE 2.1-1. SENSE WINDINGS

2.1.02 Strobe Pulses

The strobe (sample) pulse is a timed pulse used to determine which portion of the signal on the sense winding is amplified in the sense amplifiers. Any time that a core is read, noise is generated on the sense winding. By proper timing of the strobe pulse, the portion of the sense output which gives the greatest noise-free output is selected for amplification. Figure 2.1-2 shows typical strobe time when reading a one from a ferrite core.

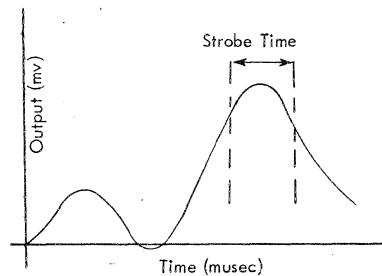


FIGURE 2.1-2. SENSE OUTPUT

The timing of strobe pulses is one of the most critical timings in the machine. To assure that they occur at the proper time in relation to the X and Y drive line current, a special strobe generator circuit is used (Figure 2.1-3).

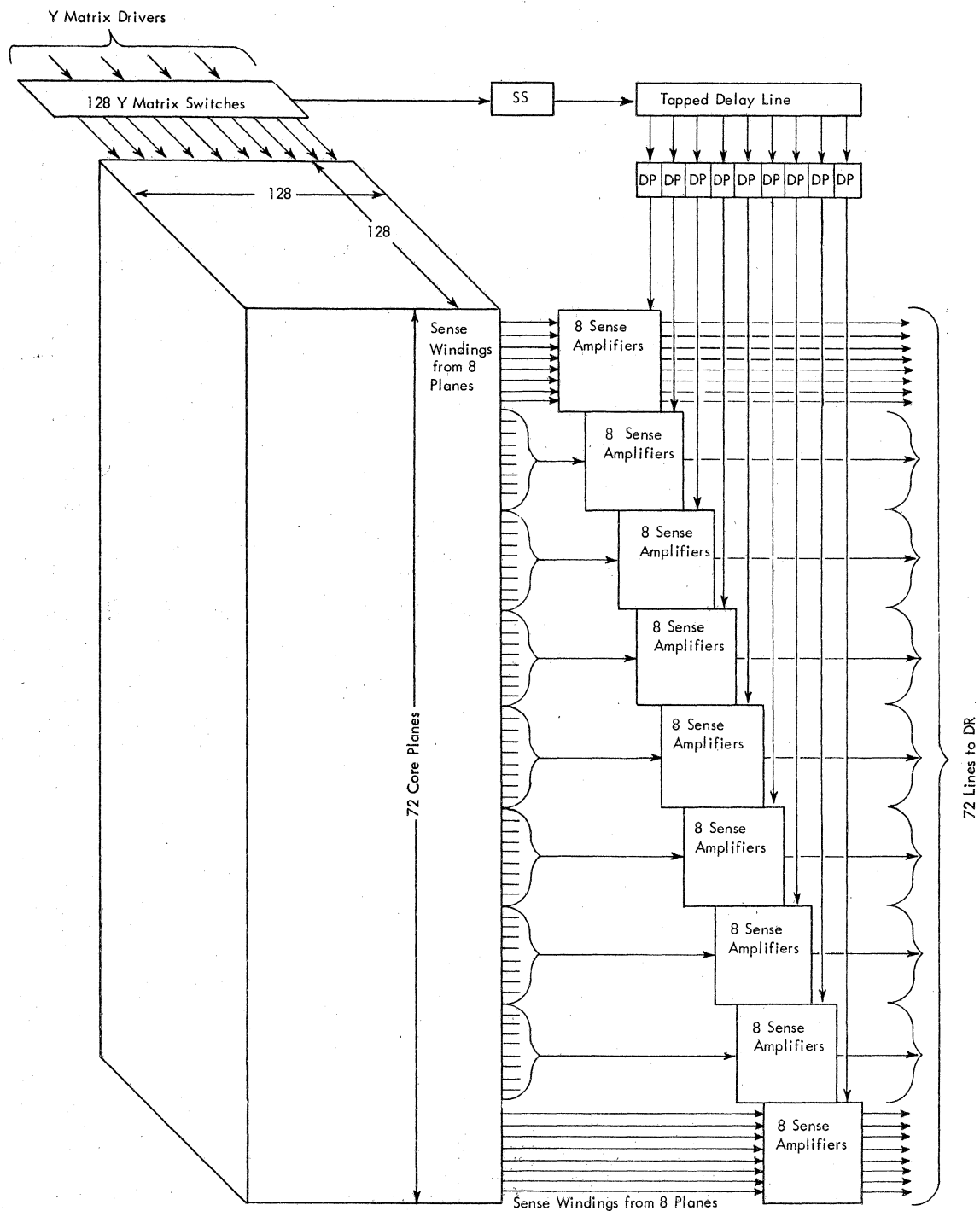


FIGURE 2.1-3. STROBE PULSE GENERATION

The impulse to the strobe generator is taken from a single winding through the matrix switches for the Y drive lines. Using this impulse assures correct timing between sense output and the strobe pulse. Another factor in strobe timing is the time it takes the drive current in the X and Y lines to travel through the 72 planes. Ideally, each plane would have a separate strobe pulse. Because this is impractical, the sense amplifiers are strobed in groups of eight. There are nine, time-staggered, strobe timing pulses. The strobe generator circuit uses a tapped delay line which gives nine outputs, evenly spaced in time, to correspond to the progression of sense outputs from the array.

2.1.03 Z (Inhibit) Drive Lines

The Z, or inhibit, lines are wound as shown in Figure 2.1-4.

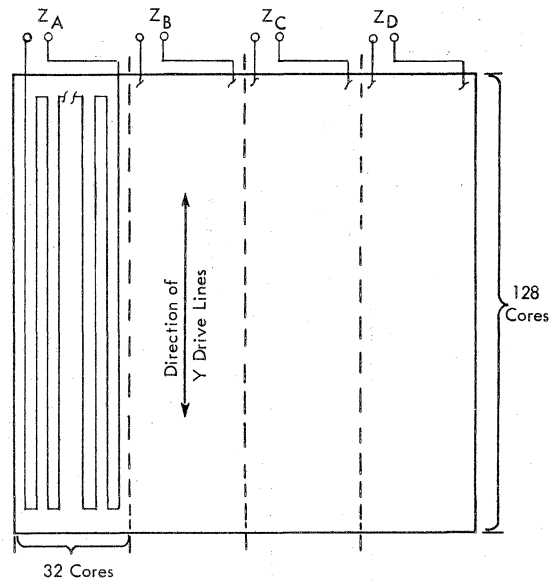


FIGURE 2.1-4. INHIBIT WINDINGS

Like the sense winding, the Z winding is segmented into four windings per plane, with a Z driver for each segment. Segmenting the Z winding reduces delay and reduces the build-up of half-select back voltage.

When a plane is inhibited, it is necessary to turn on only the Z driver in the segment of the plane that is addressed. There are four groups of 72 Z drivers, and each of the four groups is divided into five timed groups (Figure 2.1-5).

Dividing the Z drivers into groups serves two purposes:

1. If a word with all 0's were to be stored, the sudden current drain on the voltage supply would be so great that it would cause degeneration of some driver outputs. By using groups of 14 and 15 drivers at a time, this degeneration is prevented.
2. Staggering the Z drivers gives better coincidence of X, Y, and Z currents, which helps shorten the memory cycle.

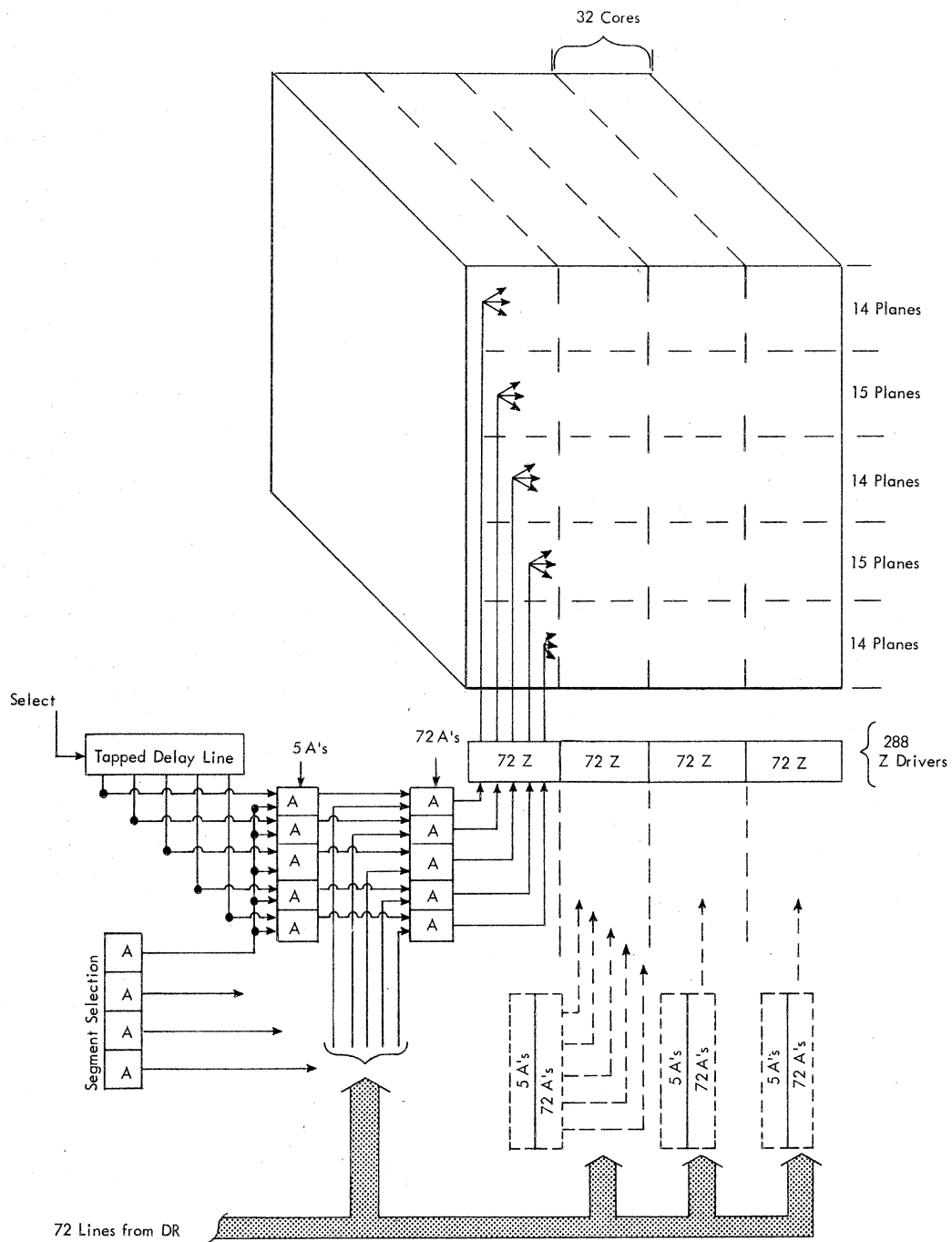


FIGURE 2.1-5. Z DRIVER SELECTION

2.1.04 Matrix Switches

The matrix switches are mounted in the first four planes of the core array. With both X and Y lines, 256 drivers are required. Because only 64 switches are in a frame, four frames of matrix switches are required. Sides B and D of Figure 2.1-6 are Y drive switches; sides A and C are X drive. Tables for determining which switch core is conducting are included with address decoding (Section 3.3.04). Input current to a matrix switch is 360 ma, output current is 585 ma.

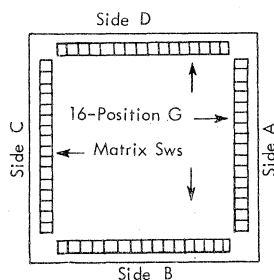


FIGURE 2.1-6. TOP VIEW OF G MATRIX SWITCH PLANE

2.2.00 NOISE REDUCTION

Unwanted noise is inherent in any ferrite core array. Major causes of noise are induced voltages and noise from the ferrite cores themselves. No core remains completely saturated and half-select current moves the flux state slightly. The change in the flux state can be either toward or away from saturation.

If the core (Figure 2.2-1) is at flux state D, half-read current would move it to point E, inducing a voltage proportional to ΔB_2 in the sense winding. If the core had been at point A, half-read current would move it to point G, inducing a similar but smaller (ΔB_4) voltage in the sense winding. Either voltage is small compared to that induced by reading a 1 from the fully-selected core (ΔB_1) but, if the output from all 254 half-selected cores in the plane were added together, the effect would be troublesome. Since a half-selected 1 causes more flux change than a half-selected 0, the effect would be especially bad while trying to read a 0 if all the half-selected cores contain 1's.

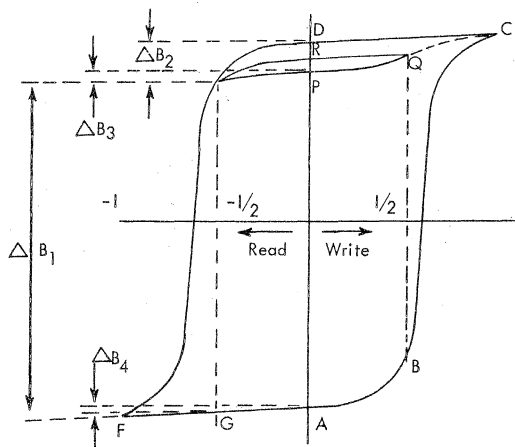


FIGURE 2.2-1. EFFECTS OF HALF-SELECT CURRENT

The greatest noise, ΔB_2 , is on the first read half-select, following the writing of a 1. When the core is half-selected in the write direction, the operating point moves to point Q instead of C. On subsequent half-select cycles, the core follows the path Q, R, E, and E, P, Q (the resultant flux change being ΔB_3 , which is considerably smaller than ΔB_2).

A similar condition exists between points G, A, and B on repeated half-select cycles. This condition is omitted since the greatest change in flux would be when the core is going in the write direction and the sense windings are not used.

Several means are used to reduce unwanted noise to the lowest possible level:

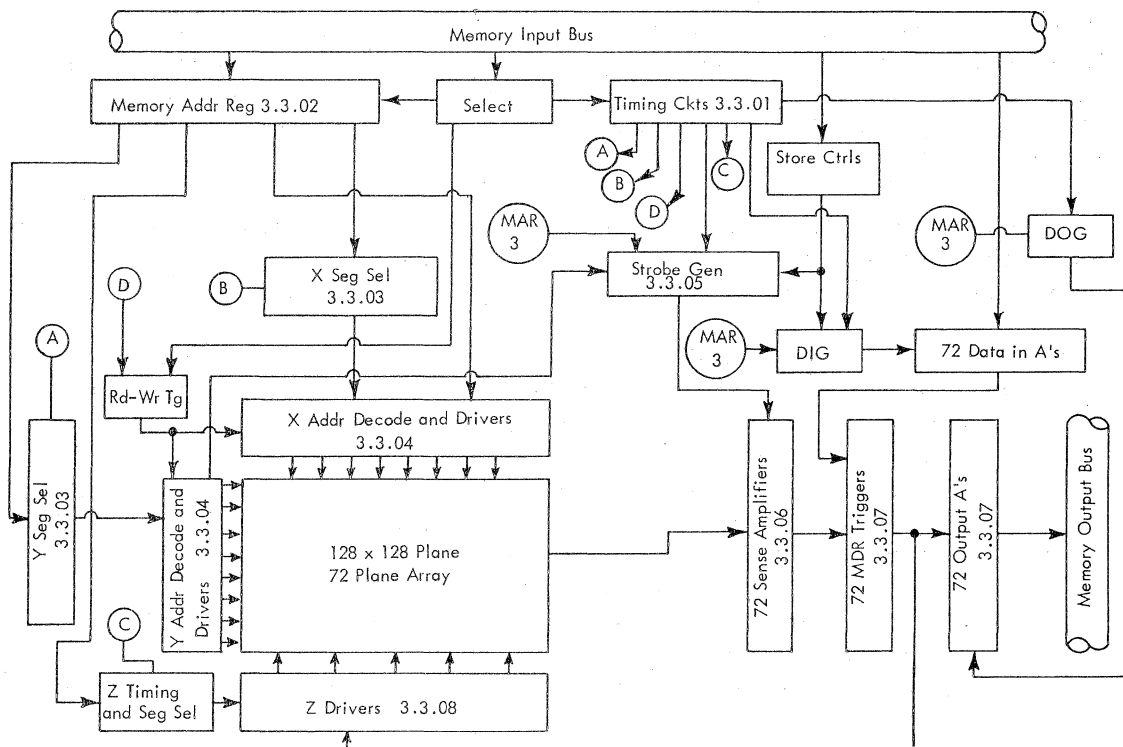
1. Sense windings are wound in a figure-eight pattern to allow cancellation of half-select noise. They are also segmented to reduce the number of half-select cores felt by any one winding.
2. Drive current through the Y drive lines is delayed so the half-select noise due to X drivers has settled down before the Y drive lines are impulsed.
3. Sense and Z windings are perpendicular to each other. Even though the sense winding is not used during Z driver time, the induced voltage on the sense winding could prevent the sense amplifiers from recovering before the next read time.
4. The physical arrangement of the core plane has current flowing in alternate directions for both X and Y drive lines, keeping induced voltages between cores and lines to a minimum.
5. Controlling the temperature of cores keeps half-select voltage from becoming greater because of a change in the hysteresis curve.
6. All X and Y drive lines are skewed to reduce self-inductance in the drive lines. The array is skewed in groups of 32 rows of cores; groups of 32 were chosen because the Z and sense windings are segmented in groups of 32 rows of cores. Reference pages in core storage systems show the location of drive lines, for any plane, by address.

2.3.00 WORST AND BEST PATTERN

A worst pattern is a bit configuration, in a core plane, whose half-select noise creates the greatest opposition to a desired pulse. In this case the half-select noise adds to the 0 or subtracts from the 1 which is trying to be read from the selected cores. The opposite condition produces a best pattern.

2.4.00 WORD PATTERN IN CORE ARRAY (7090)

With a 72-plane core array and a system that uses a 36-bit word, any address within the array contains two 36-bit words. The top section of the array, planes 0-35, is one word; planes 36-71 contain the other word. The two words are a mirror image of each other; i.e., planes 0 and 71 are used for sign position; and planes 35 and 36 are the 35th bit position for each word. The use of a mirror image was chosen for simplicity of circuit design to cover instructions that alter only a portion of a word; i.e., store tag, store decrement, store prefix, and store address.



A = Y Driver Timing Pulse
 B = X Driver Timing Pulse
 C = Z Driver Timing Pulse
 D = Rd-Wr Trigger Timing

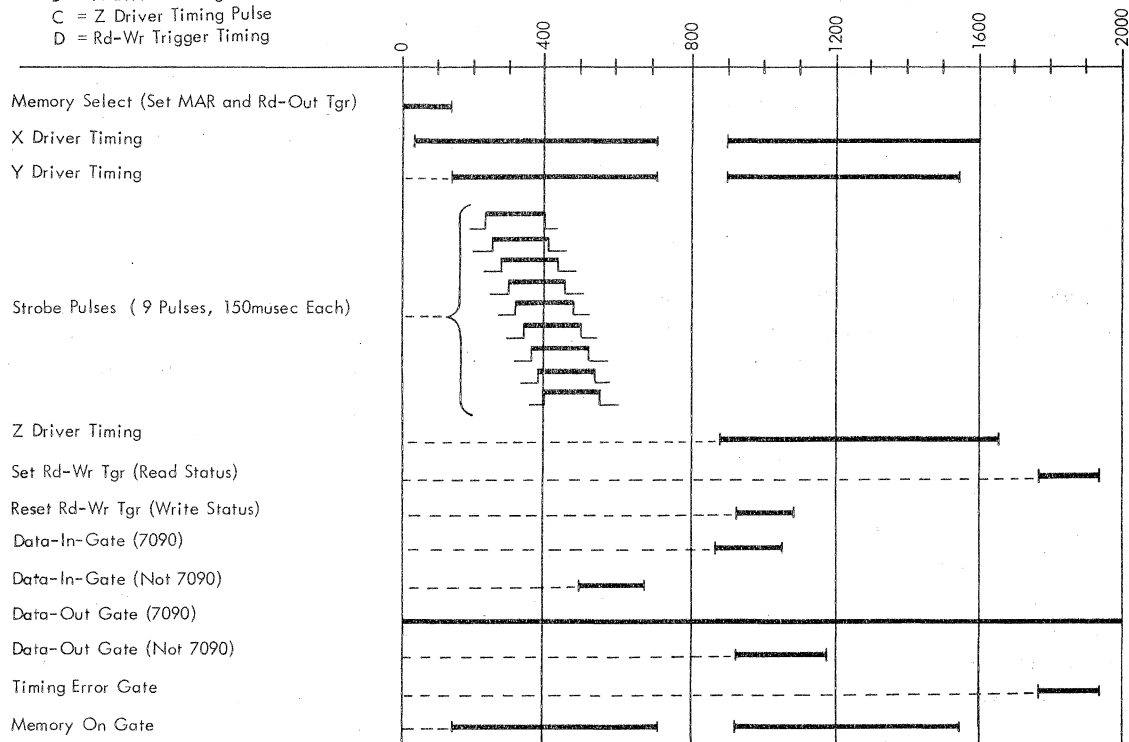


FIGURE 3.1-1. CORE STORAGE LOGIC

3.0.00 CORE READ-STORE OPERATIONS

3.1.00 READ OPERATIONS

To read out of core storage and place the information on the output bus, a core in each plane must be selected and read. This information is put on the output bus, then the same information is replaced in the cores (Figure 3.1-1).

Remember that the information that is read from the core array contains 72 bits, since it is a 72-plane array. All 72 bits are read into the data register and from the data register the 72 bits are put on the output bus.

In 7090 systems a selection must be made to determine which of the two 36-bit words in the data register are put on the output bus. Selection is determined by the presence or absence of a bit in position 3 of the address register. The absence of a bit in position 3 selects the word from core planes 0-35. A bit in position 3 selects the word from core planes 36-72.

3.1.01 Read Cycle

During the first half of any machine cycle in which core storage is used, one core in each plane is impulsed with X and Y drive current in the read direction (This sets all selected cores to 0.). See Figures 3.1-1 and 3.1-2. This portion of a machine cycle is called a read cycle and information is read out of the ferrite cores.

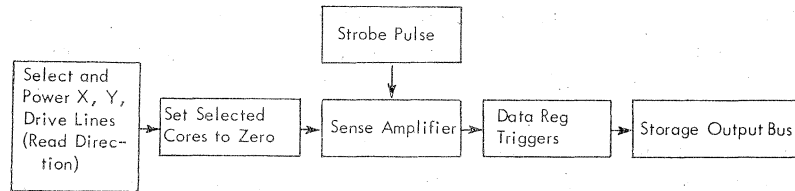


FIGURE 3.1-2. READ CYCLE

In Figure 3.1-1 the read line of read or write control is up throughout the read cycle. If there is an output from the sense winding, it is conditioned at the output stage of the sense amplifier by a strobe pulse, which allows the pulse to set a trigger in the data register. The strobe pulse is a short pulse that occurs every read cycle. If there had been no output from the sense winding, the data register (DR) trigger would have remained off, indicating that a 0 was read.

The output of the data register is gated at the output with circuits that determine which of the two words read out is to be fed to the output bus.

Once the read cycle is performed, the information in the core has been destroyed and must be replaced. Because the DR triggers still have the information which was read from the cores, the DR can be used to control a rewrite operation.

3.1.02 Rewrite Cycle

During the last part of any operation, the X and Y drive lines are again impulsed but in the opposite, or write, direction (See Figures 3.1-1 and 3.1-3). Write current would cause each of the selected cores to flip to a 1 status. The Z (inhibit) drivers determine which cores are allowed to flip to a 1 status. The Z drivers, fed from the data register triggers, cancel Y drive current in those cores which are to remain in the 0 state. If a data register trigger is off (a 0 had been in the core originally), the Z driver is free to conduct. Any data register triggers that are on, block the Z drivers, and the X and the Y drive currents set the selected cores to a 1 status.

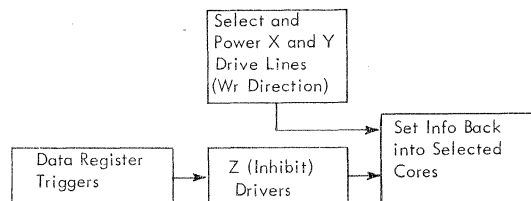


FIGURE 3.1-3. REWRITE CYCLE

Notice that in the rewrite cycle, X, Y, and Z drivers are used. The X and Y drivers try to write 1's in all selected cores and the Z drivers determine which of the selected cores are allowed to flip to a 1 status. The Z drivers can select a core because half-select current does not flip a core.

3.2.00 STORE OPERATIONS

To place new information into core storage:

1. Read the selected cores (Set them to a 0 status.).
2. Set the data register triggers with the new information from the input bus.
3. Write the new information (as in rewrite).

3.2.01 Read Cycle

As in every core cycle, the first half of the cycle is a read cycle during which an X and Y drive line is impulsed with read current to set all selected cores to zero. See Figures 3.1-1 and 3.2-1.

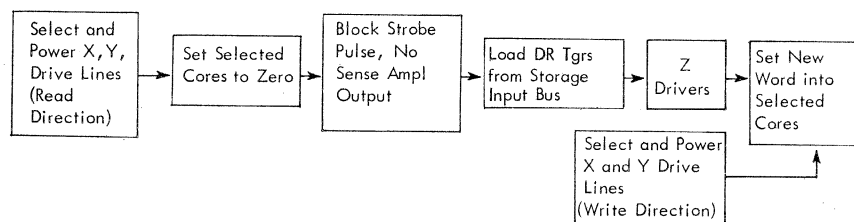


FIGURE 3.2-1. OPERATIONS TO WRITE A NEW WORD INTO STORAGE

In a store operation, the strobe pulse is prevented from reaching the sense amplifiers. With no strobe pulse, no information is gated from the sense amplifiers to the data register triggers. The read portion of the store operation has, therefore, destroyed the old, unwanted, information.

The new information to be placed into storage is gated to the data register triggers from the storage input bus through AND circuits that are gated by an input control line.

3.2.02 Rewrite Cycle

The rest of the cycle is now the same as the rewrite portion of a read operation (Section 3.1.02).

3.2.03 Store Partial Word (7090)

It is possible to store only a portion of a word. Operations which store only a portion of a word are:

1. Store prefix -- stores bits 0, 1, and 2.
2. Store decrement -- stores bits 3 through 17.
3. Store tag -- stores bits 18, 19, and 20.
4. Store address -- stores bits 21 through 35.

These operations have the following sequence:

1. Read the selected cores (Set them all to 0.).
2. Kill strobe pulse to sense amplifiers 0, 1, and 2.
3. Read new information from the input bus for data register positions 0, 1, and 2.
4. Rewrite the selected cores.

Notice that the operation is identical to storing a complete word, except that only a section of the strobe pulse is killed and the corresponding section of the new word is allowed to read into the data register triggers.

3.3.00 CIRCUIT LOGIC

The previous section covered logically how a word is read from storage or is stored. Now, each of the logic blocks is discussed separately and in greater detail. In Figure 3.1-1, each major block contains a section number. The section indicated expands that particular logic block and shows how it accomplishes its purpose.

3.3.01 Memory Timing Circuits

Timing circuits are used to control all operations of the core storage unit in proper sequence and time. The unit is asynchronous, because it initiates all of its own timing pulses.

Any core storage operation must be started by selecting the unit. The rise of the memory select line is the basis for all timings within the unit.

The timing circuits consist of a group of delay units fed from the memory select line. By choosing delay units of proper duration, a pulse may be obtained at any time throughout the core storage unit cycle. Gate pulses can be obtained by using one delay line to turn on a trigger and a second delay line to turn off the trigger.

Figure 3.3-1 illustrates the use of delay lines to develop a timed pulse and a gate. The timed data out gate comes up 930 millimicroseconds (musec) after the rise of memory select. Two delay units are used in series: the first unit is a fixed delay; the delay time of the second unit can be varied. Timing of the second delay unit cards may be varied for exact timing by changing the card cap cut (Card timing can be changed in increments of 5 musec to 6 musec.). The Z timing gate shown in Figure 3.3-1 begins when the trigger is turned on 870 musec after the rise of memory select. The trigger is turned off 1650 musec after the rise of memory select. The length of the Z timing gate is therefore 780 musec. All timings and gates are developed in a similar fashion. The time shown in the Dly blocks is the actual time delay used in the circuits.

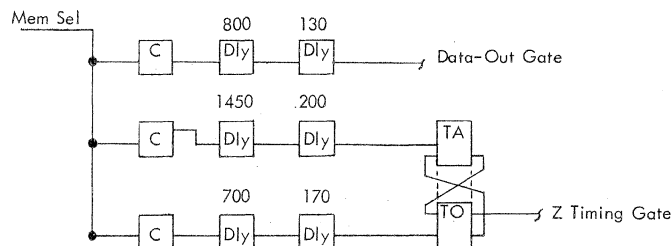


FIGURE 3.3-1. TIMED PULSE AND GATE DEVELOPMENT

Figure 3.1-1 gives the major timings of the core storage unit. A discussion of how each timed pulse is used is covered in the discussion of the particular circuit.

3.3.02 Memory Address Register

The memory address register (MAR) contains the address of the selected core storage word. Information being fed to the MAR is conditioned by the memory select line, which both gates and times the MAR input.

The MAR is a form of latch which retains information. If, on successive memory selects, a MAR position receives a one bit, the output of the register never drops or alters. When a memory select is received without a one bit on the MAR line, the register is altered so the output level is reversed; this condition again exists until a memory select is received with a one bit on the MAR line.

Figure 3.3-2 is a block diagram of a MAR position. AND_1 is the input to the register. Note that AND_1 has a supervisory input; as a result the in-phase output will follow the MAR input line when the memory select line is up. A positive memory select pulse with a negative pulse on the MAR line represents a 1 being read into the register. Reading in a zero would condition both input lines to AND_1 positive.

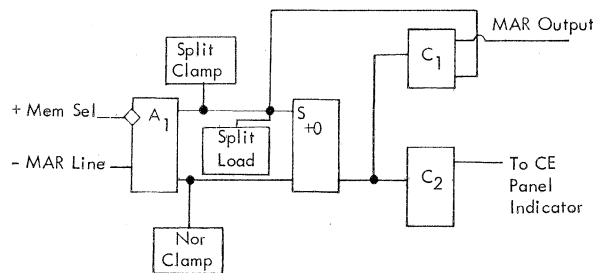


FIGURE 3.3-2. MEMORY ADDRESS REGISTER LOGIC

The input to the OR circuit from the out-of-phase output of AND_1 is marked with an "S" (split load). The split load causes the in-phase output of the OR circuit to follow the split load input. To read a 1 into the register: memory select is up, the MAR line is down, the out-of-phase output of AND_1 is up causing an up level out of the OR circuit which is latched by feeding back through C_1 . When a zero is read into the register: both the memory select and MAR lines are up, the out-of-phase output of AND_1 is down, the output of the OR circuit is down which is again latched by feeding back through C_1 .

When the MAR contains a 1, the MAR output line has a down level; conversely a 0 status causes an up level on the MAR output line. The C_2 output feeds an indicator lamp on the CE panel.

3.3.03 X and Y Segment Selection

Segment selection uses three MAR outputs to determine which group of matrix switches is allowed to conduct, producing X or Y drive line current. Recall that a 128 x 128 core plane is used. Because matrix switches are manufactured in groups of 16 switches, eight groups are required to develop 128 drive lines. Segment

selection uses three MAR positions to develop eight segment gates. The address decoding circuits condition drivers to select one switch core in each of the eight segments; the segment gate selects which of the eight groups are used to produce drive line current.

Figure 3.3-3 illustrates development of the eight segment gates. Because the segment gates for either X or Y lines are similar, the input lines are labeled A, B, and C. The X segment gates are developed from MAR positions 15, 16, and 17, while Y segment gates use MAR positions 8, 9, and 10.

Outputs from the MAR are fed through converters which have both in-phase and out-of-phase output lines. A group of eight minus AND (-AND) circuits are used to combine the six converter outputs into the different segments.

A line labeled C indicates that the line has an up-level when there is a bit in MAR position C. A line labeled $\bar{C}$ indicates that the line has an up-level when there is not a bit in MAR position C.

Assume that a bit is in MAR A and C. On the output lines of the converters, lines A, $\bar{B}$, and C have an up-level; conversely lines $\bar{A}$, B, and $\bar{C}$ have a down-level. Since the lines are feeding a -AND circuit, lines $\bar{A}$, B, and $\bar{C}$ are the controlling lines, and a -A must be found which uses the three lines. The -AND for segment 5 satisfies the required conditions. The segment line selected is the octal value of the MAR positions 8, 9, and 10 or 15, 16, and 17.

The -AND circuits are further conditioned by a driver timing pulse. The driver timing pulse is a timing gate which conditions the -AND circuits during the read portion of the cycle and again during the write portion of the cycle. The timing pulse also establishes the exact time when X and Y drive line current flows. Timing relationships of X and Y driver timings are shown on Figure 3.1-1. Note that X drive line current is developed before Y drive line current.

The sense winding is parallel to the X drive lines so some induced noise is inherent on the sense winding. Delaying the Y drive line current allows the noise on the sense winding to decay before the ferrite cores are flipped, reducing noise to the sense amplifiers.

3.3.04 X and Y Address Decoding

Address decoding uses four MAR outputs plus the read or write cycle trigger output to condition drivers which, in conjunction with segment gating, produce drive current in one X or Y drive line.

Because the matrix switches are manufactured in groups of 16, it requires 16 drive lines to cause one switch core to flip during the read portion of the cycle. Another set of 16 must conduct to produce current in the opposite direction during the write portion of the cycle. Therefore, a total of 32 lines must conduct during each core cycle. The read-write trigger is the one factor which changes, causing the reversal in drive line current.

Figure 3.3-4 is a schematic diagram illustrating the method used to develop the 32 matrix switch core drivers.

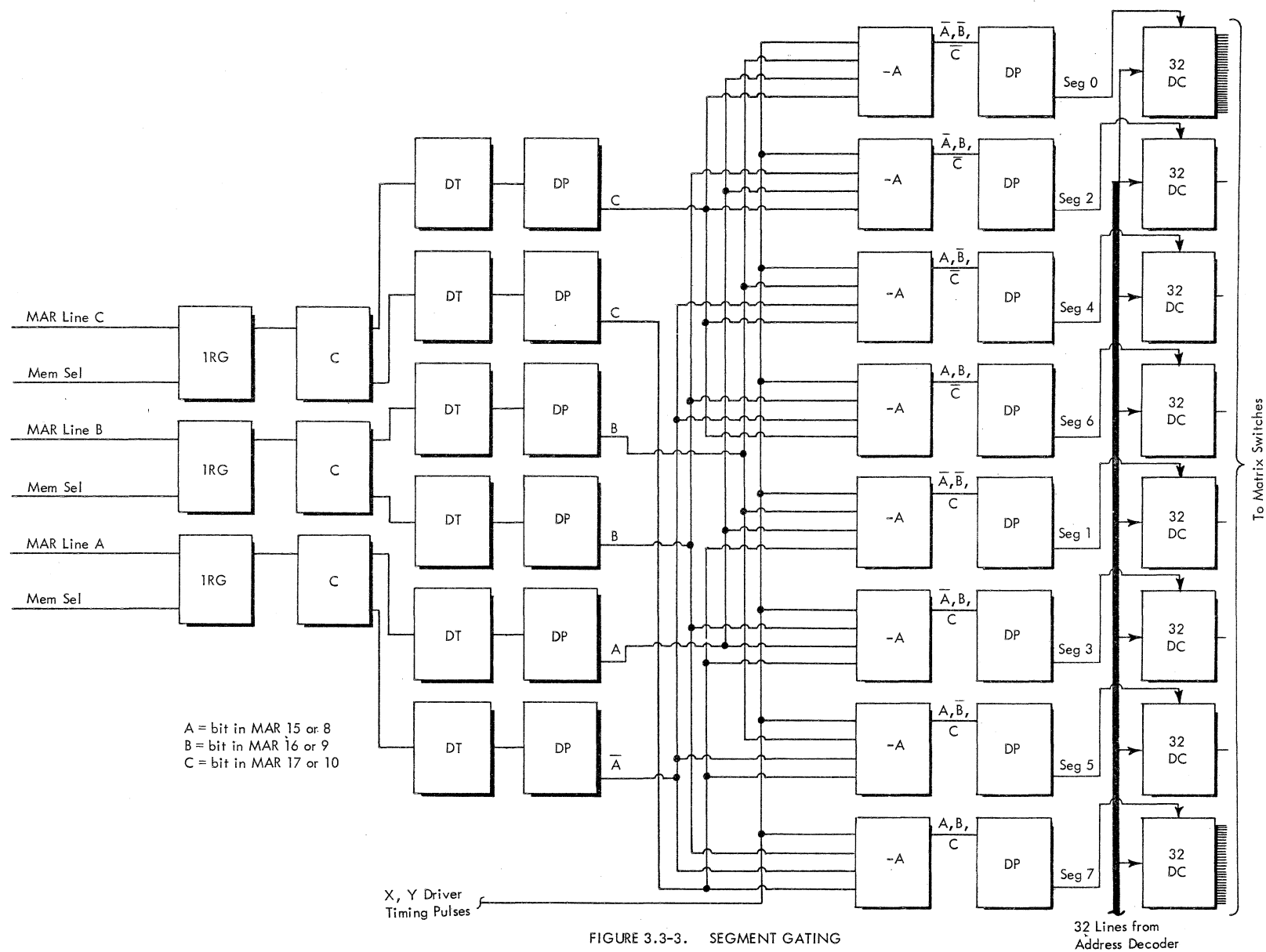


FIGURE 3.3-3. SEGMENT GATING

Assume a bit is in MAR positions A and C during the read portion of a core storage cycle. Converter output lines A, $\bar{B}$, C, $\bar{D}$, and R have an up-level; lines $\bar{A}$, B, $\bar{C}$, D, and $\bar{R}$ are down. The converter output lines feed eight minus exclusive OR circuits (-OE) and two converters. Figure 3.3-5 illustrates characteristics of -OE and +OE circuits.

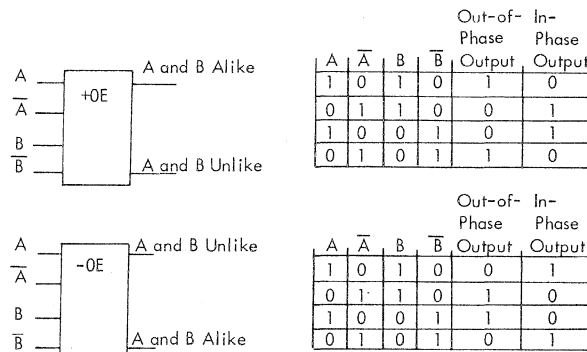


FIGURE 3.3-5. EXCLUSIVE OR CHARACTERISTICS

The symbol ∇ means "exclusive OR;" therefore, $R \nabla A$ for an output means that either input, R or A, is an up-level, but not both. The not function, $\bar{R} \nabla \bar{A}$ indicates that R and A or $\bar{R}$ and $\bar{A}$ both have an up-level on the input to the circuit,

The lines with an up-level to $-OE_1$ (Figure 3.3-4) are A and R; therefore, the up-level output is the in-phase output line marked $R \nabla A$. On $-OE_2$, the up-level is the out-of-phase line marked $R \nabla B$ because the up-level inputs are R and $\bar{B}$. Similar logic determines which line is up for the remaining -OE and C circuits.

At this point, the four MAR inputs and the read or write trigger output have been expanded to ten complementary, or a total of 20, lines. The 20 lines, called first level memory address drivers (MAD), are further combined through C's and +OE's to develop 16 complementary lines or a total of 32 lines which condition core drivers (DC) in each of the eight segments. The input to a core driver is an AND circuit; one leg of the AND circuit is conditioned from the segment gating, the other from address decoding.

Output lines to the core drivers are labeled so that the output lines with an up-level can be determined from a knowledge of which MAR positions have a bit in them. Using the previous example, where there was a bit in MAR positions A and C, check the +OE feeding C4. The inputs to the +OE are an up-level R and an up-level $A \nabla B$ from $-OE_3$. The up-level output of C4 is $R \nabla (A \nabla B)$ because both R and $(A \nabla B)$ are up. The same conclusion could have been reached by considering only the MAR outputs. The original conditions gave us R; $(A \nabla B)$ requires that A or B be up, but not both, which is the case; therefore, both R and $(A \nabla B)$ are up-levels. The notation $R \nabla (A \nabla B)$ is used to denote that both R and $(A \nabla B)$ are up. This is the same line that was developed using the inputs to the +OE circuit. Notice also that when the core storage unit is in the write portion of the cycle, the complement line out of C4 is up. In this case $(A \nabla B)$ is an up-level, but R is a down-level; therefore, $R \nabla (A \nabla B)$ is the line with the up-level. The same condition holds true for all of the driver lines; one line is up during the read portion of the cycle and the complement line is up during the write portion of the cycle. It is this reversal that conditions the core drivers so X and Y drive line current is in one direction for a read cycle and in the opposite direction for a write cycle.

With 16 core drivers feeding a selected segment during read time, which matrix switch is going to produce the X or Y drive line current? The matrix switch selected depends on how they are wired. The location of the impulsed matrix switch can be located using Figure 3.3-6.

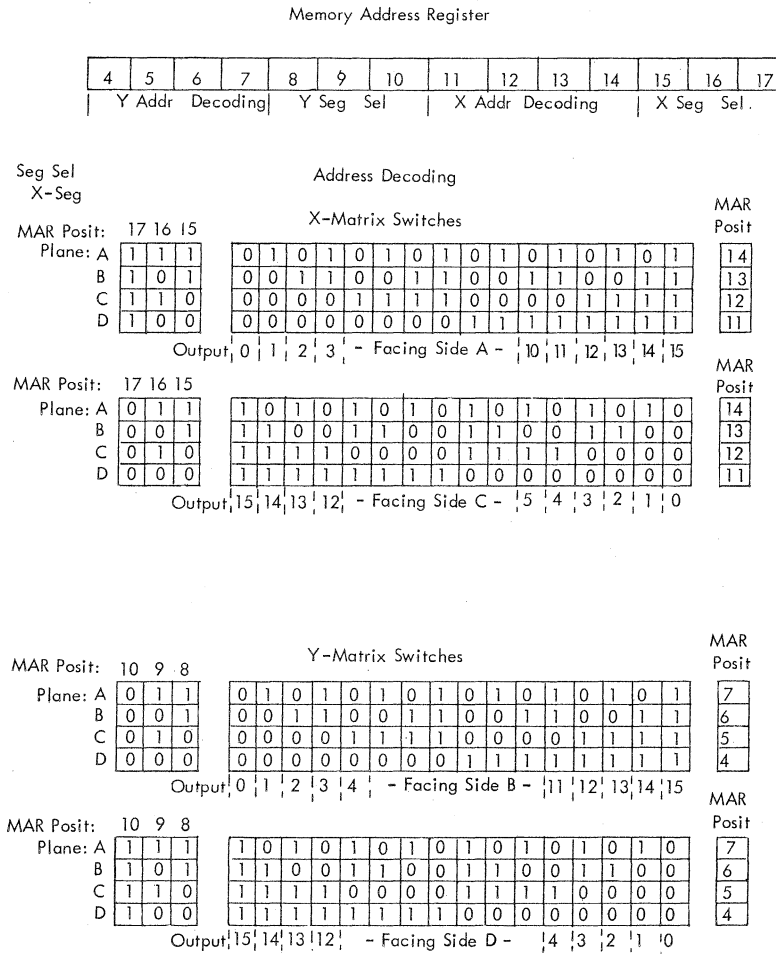


FIGURE 3.3-6. SELECTED MATRIX SWITCH LOCATION

Assume the MAR contains all 0's. To determine which X segment (group of 16 matrix switches) is conditioned, find the block under segment selection where MAR positions 15, 16, and 17 are all 0. The chart shows that this segment is located in plane D on side C of the array. Now locate the vertical column opposite the selected segment in the chart under Address Decoding that has 0's for MAR positions 11, 12, 13, and 14. Matrix switch 0 is the actual physical location, in the array, of the impulsed switch core. The impulsed matrix switch for any address may be determined by locating the bit configuration in the charts.

Reference pages in core storage Systems list test points to check matrix switch output by address.

3.3.05 Strobe Generation

The strobe pulse is a timed pulse which samples, or gates, the output of the sense amplifiers.

To obtain the correct timing of the strobe pulse, a timing pulse is used in conjunction with an output from the Y matrix switches. The timing pulse must be used for gating because the matrix switches produce an output for both the read and write portions of the cycle.

Figure 3.3-7 is a logic diagram of the circuit which determines the initial timing and width of the strobe pulse. The circuit in Figure 3.3-7 serves as a single shot; the delay unit determines the width of the output strobe pulse. The waveforms shown in Figure 3.3-7 show inputs and outputs of the AND circuits. Notice that the only time a positive output can be obtained from the minus AND circuit is while both inputs are down. This duration is determined by the amount of delay of the Dly₂ unit. The plus AND circuit gates the output to allow a strobe pulse only during a read cycle. Dly₁ is used to obtain close, or fine, timing of the strobe pulse.

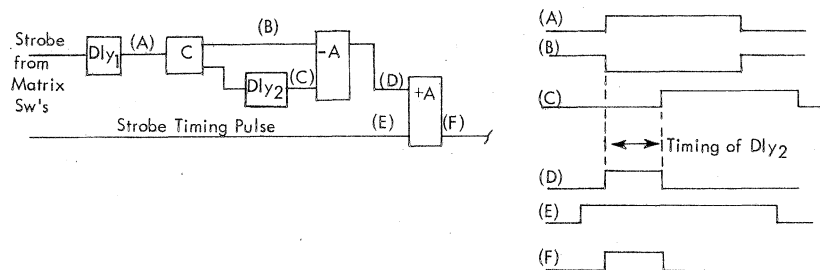


FIGURE 3.3-7. STROBE TIMING AND WIDTH DEVELOPMENT

The gated strobe pulse from the matrix switches feeds a group of nine delay units, which determine the timing of the strobe pulse to the individual sense amplifiers.

Figure 3.3-8 illustrates the conditioning of strobe pulses. Notice that the strobe timing pulse is gated through AND circuits before going to the sense amplifiers.

If the core storage operation is a read operation, read out, through the +OR circuits, conditions the +AND circuits so all 72 sense amplifiers are strobed.

On store operations, the strobe pulse is blocked so the new data to the data register can be taken from memory data bus in (MDBI). Blocking of the strobe pulse is accomplished as follows:

1. On store operations, read out is down.
2. On a store operation all store partial word lines come up.
3. Store operations in not 7090 systems have the same operation as 7090 systems, except that all 72 outputs are blocked because both MAR 3 lines are up.

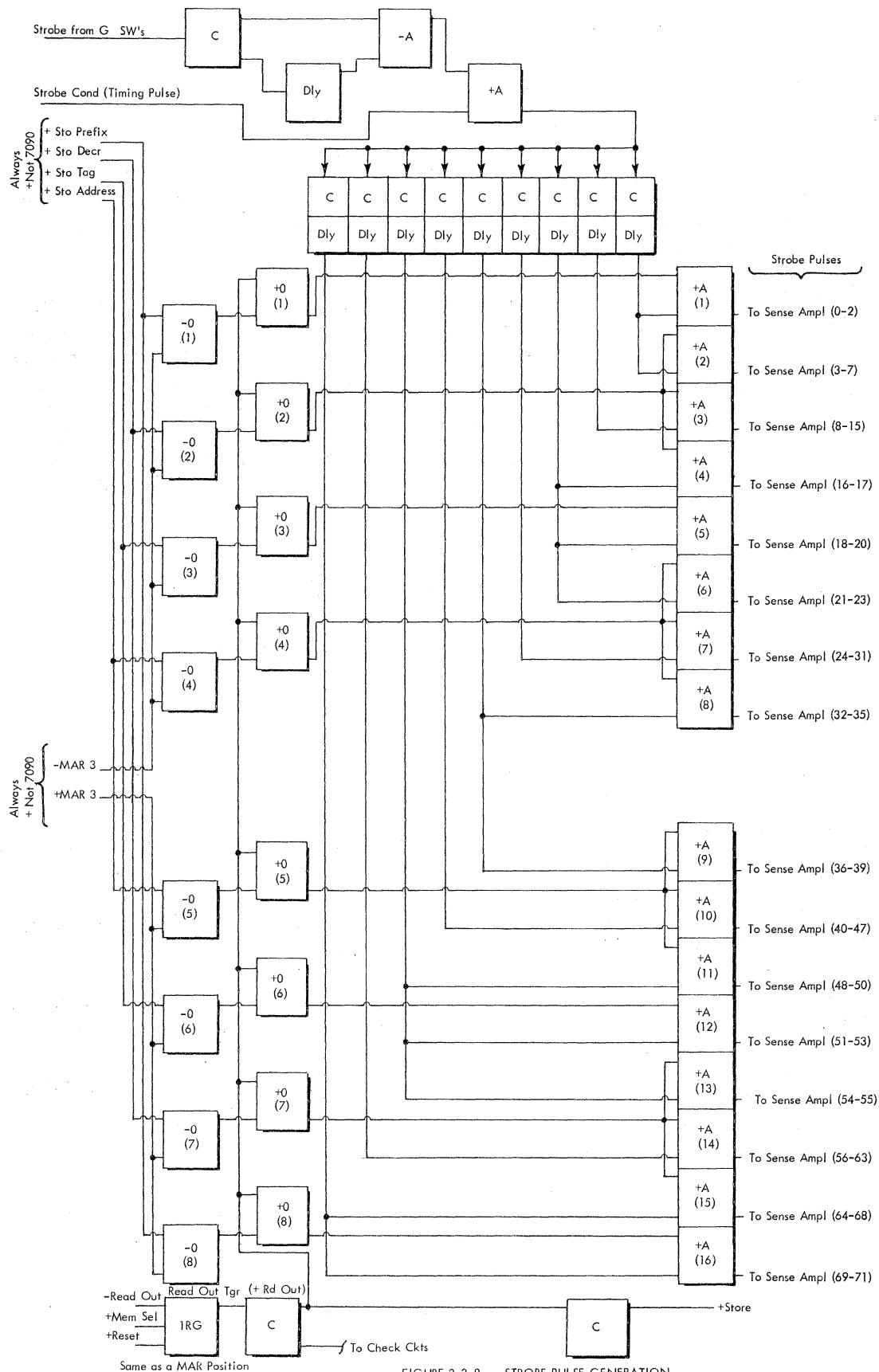


FIGURE 3.3-8. STROBE PULSE GENERATION

Assuming that the addressed word is in the low-order section of the core (addresses 00000 through 37777), the MAR 3 line to -OR circuits 1-4 is up. Therefore, the out-of-phase output of -OR circuits 1-4 is down; read-out is down, so the output of +OR circuits 1-4 is down. The down outputs of +OR circuits 1-4 block +AND circuits 1-8 so no strobe pulse can reach sense amplifiers 1-35. Sense amplifiers 36-71 in 7090 systems receive a strobe pulse because the out-of-phase output of -OR circuits 5-8 is up, which takes an up-level to the input of +AND circuits 9-16.

On store partial word instructions, e.g., store prefix, only store prefix comes up. The other lines, store decrement, store tag, and store address, are down. The result is that all sense amplifiers, except 0-2, are strobed to allow their outputs to set the data register triggers.

OR to Storage (7090)

On an OR to Storage (ORS) operation, the CPU initiates a memory store cycle. As in any store operation, the data in gate will gate data from the memory data bus in to the memory data register triggers. An ORS line allows the sense amplifiers to be strobed even though the core storage unit is in a store operation. Thus, the MDR triggers will be turned on with the data from the MDBI or from the sense amplifiers.

Only one special ORS line is used to force an output from the sense amplifiers. The store partial word lines of Figure 3.3-8 will be held down by an ORS control line on Systems 1.13.00.1. When the store partial word lines of Figure 3.3-8 are down, the -OR₍₁₋₈₎ circuits have an up output, through the +OR₍₁₋₈₎ to the strobe generator output AND circuits, allowing all sense amplifiers to be strobed. The output of the sense amplifiers is not gated into the MDR triggers. Therefore, any sense amplifier output will turn on the corresponding MDR trigger. Data to set the MDR triggers from the MDBI are identical to a normal store operation.

3.3.06 Sense Amplifier

The sense amplifier receives and amplifies signals from the sense windings. Recall that each plane has four separate sense windings. Each of the four sense windings (Figure 3.3-9) per plane has its own differential amplifier. All four outputs are OR'ed together at the emitter follower. The output of the emitter follower is anything that is on the sense windings: noise, data pulses, and so on. The strobe-gated amplifier is the circuit which determines what appears at the output of the sense amplifier. The strobe pulse gates the amplifier so it can conduct only while the strobe pulse is available. The output stage of the sense amplifier is a level setter which feeds directly into the memory data register triggers. The level setter is required because of special voltages and levels used in the sense amplifier circuits.

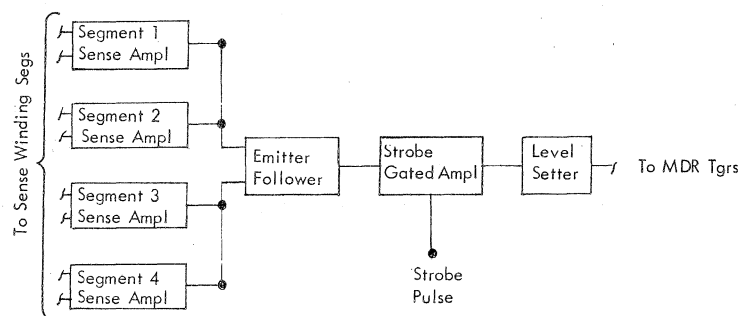


FIGURE 3.3-9. SENSE AMPLIFIER

3.3.07 Memory Data Register

The memory data register (MDR) is the output register for the core storage unit. Figure 3.3-10 is a logic diagram of the MDR and its controls. A block diagram is also shown for one MDR position. Note that the MDR logic block contains an input and an output AND circuit plus a trigger. The MDR input AND circuit uses a data-in gate (DIG) to gate data from the memory data bus in to the MDR trigger. The MDR output AND circuit uses a data-out gate (DOG) to gate data from the MDR trigger to the memory data bus out (MDBO). The data-in and data-out gates are timed pulses which gate the input and output of the MDR. Controls for the MDR are described with each type of operation.

Storage Read-Out Operation (7090)

On read-out operations, 72 outputs are read from the array, through the sense amplifiers and are fed directly into the MDR triggers. The MDR feeds 36 bits to the output bus and all 72 bits to the Z drivers.

Which 36 bits are read out to the MDBO is determined by MAR 3. If there is no bit in MAR 3, its input to -AND_{10} is down. The data-out gate (DOG) is a gating pulse which determines when the MDR triggers are read out. When the DOG goes negative, an up-level is available from the -AND_9 out-of-phase output to the MDR (0-35) output AND circuits putting 36 bits of information on the MDBO.

Storage Read-Out Operation (Not 7090)

During read-out operations, 72 bits are read from the array, through the sense amplifiers, and fed directly into the MDR triggers. With the rise of the data-out gate, all 72 MDR outputs are fed to the MDBO. Both MAR 3 lines are always down; therefore, when the data-in gate goes down, an up output from $\text{-AND}_{9,10}$ gates all 72 MDR output AND's to the MDBO. The (DOG) is a timed pulse from the timing circuits.

Store Operations (7090)

On a store operation, the 36 bits of information to the MDR are fed from the memory data bus in, instead of from the sense amplifiers. Recall that on a store operation, the sense amplifiers for the addressed word are not strobed. MAR 3

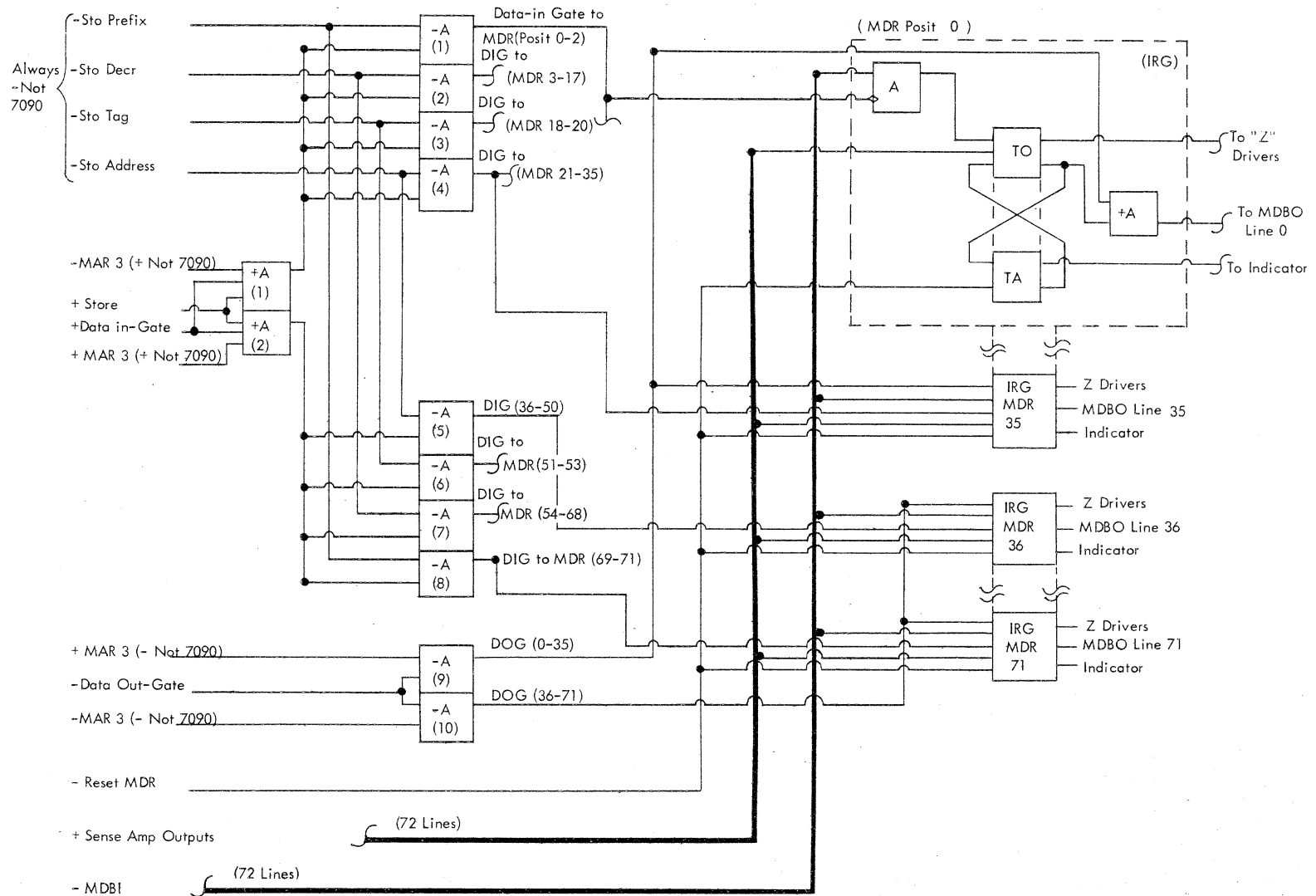


FIGURE 3.3-10. MEMORY DATA REGISTER AND CONTROLS

again decides which 36 bits are fed from the MDBI and a data-in gate determines when they read into the MDR. Assuming there is not a bit in MAR 3, the MAR 3 line to $+AND_1$ is up. The store line is up on a store operation; therefore, a down line is available from the out-of-phase output of $+AND_1$. All store partial word lines are down so an up-level is available from the out-of-phase outputs of $-AND_{1-4}$ to the input AND circuits of MDR (0-35). Notice that the DIG is a supervisory input. A down-level is required on the MDBI to obtain an up-level output to the MDR trigger. Writing the new word into the selected cores through the action of the Z drivers is the same as a rewrite cycle. No data-out gate is available during a store operation.

Store Operations (Not 7090)

During a store operation, the 72 bits of information to the MDR are fed from the MDBI, instead of from the sense amplifiers. On a store operation, the sense amplifiers are not strobed, and no data from the sense windings are gated to the MDR triggers.

The store line in Figure 3.3-10 is up, both MAR lines are always up, and all store partial word lines are always down. The data-in gate to $+AND_1$ and $+AND_2$ is the conditioning factor which determines when the information from the MDBI will set the MDR triggers. The DIG is a timed pulse from the timing circuits. Note that the DIG is a supervisory input to the MDR input AND; a down-level from the MDBI is required to obtain an up-level output to the MDR trigger.

Writing the new word that is in the MDR triggers into the selected cores is accomplished by the action of the Z drivers. The output of the MDR triggers to the Z drivers is not gated and is the same as a rewrite cycle. No DOG is available on a store operation.

Store Partial Word (7090)

On operations which store only a portion of a word, the DIG allows only a portion of a word to be read into the MDR from MDBI. Assume a store address operation. The store address line is the only one of the store partial word lines that has a down-level. As a result, $-AND_4$ is the only circuit to produce a DIG, and only the input AND circuits for MDR 21-35 are conditioned to receive information from the MDBI. The Z driver input is the same as for a store operation.

A reset line to the MDR triggers is impulsed once each memory cycle. Timing of the reset line is determined from the timing circuits. Figure 3.1-1 shows the timing relationship of the DIG, DOG, and MDR reset pulse.

3.3.08 Z Driver Selection and Timing

Z drivers serve only one function. During the rewrite cycle, any Z driver which is conducting prevents (inhibits) the selected ferrite core from being set to a 1 status.

The Z drivers are segmented so only the driver in the segment containing the selected core conducts. Z segment selection is determined from MAR positions 4 and 5. The segment is further conditioned by timing pulses, which stagger the time that Z drivers go into conduction to reduce power supply loading. Figure 3.3-11 illustrates the method used to select and time Z drivers.

Outputs from MAR positions 4 and 5 are used to develop four segment outputs: A, B, C, and D from $+AND_{(1-4)}$. Assuming both MAR 4 and MAR 5 contain a bit, the out-of-phase output of $+AND_1$ conditions $-AND_5$. Once the segment is selected, the segment gate is further conditioned by timed pulses. Memory select, through a delay unit operates a trigger, whose output times each group of Z drivers. The trigger output sets the initial time the Z drivers can go into conduction and also determines the duration of Z drive line current. The input to the trigger uses delay units to turn the trigger both on and off, forming a type of single shot.

With the down-level from segment selection and the delay unit, $-AND_5$ gates the core drivers for planes 0-13. The out-of-phase outputs from MDR 0-13 feed these same core drivers. Any core driver which has both inputs (segment gate and MDR out-of-phase output) up, conducts. The current through the Z winding cancels the Y drive line current during the rewrite cycle and prevents the selected core from being set to a 1 status.

3.3.09 Core Drivers

Core drivers are used to drive matrix switches for X and Y drive line current and to drive Z (inhibit) winding current. The core driver circuits for both X and Y drive lines and Z windings are identical except for the type of power transistor used and the collector voltage to the power transistor.

Figure 3.3-12 is a block diagram of a core driver and the driver windings. A separate drawing is made for each driver to show the winding configuration. For Z drivers, the output transistor of the core driver feeds the Z winding directly. The core drivers for X or Y drive lines drive matrix switches. Recall that 16 drivers are conducting through the group of matrix switches at one time. The secondary output of the matrix switches carries the actual X and Y drive line current.

The core driver circuit consists of an input AND circuit to gate information into the power driver which, in turn, drives a power transistor. A schematic drawing of the power transistor is shown. Note that the shield of the coaxial cable is tied to the collector supply voltage and that the driver fuse is located on the transistor card.

3.3.10 Power-On Reset

A timing reset line in core storage comes up when power is brought up on the storage unit. Note that a power on reset (Figure 3.3-13) will reset only the Rd-Wr trigger and timing circuit triggers. All registers in the core unit initiate their own reset each cycle or do not require a reset.

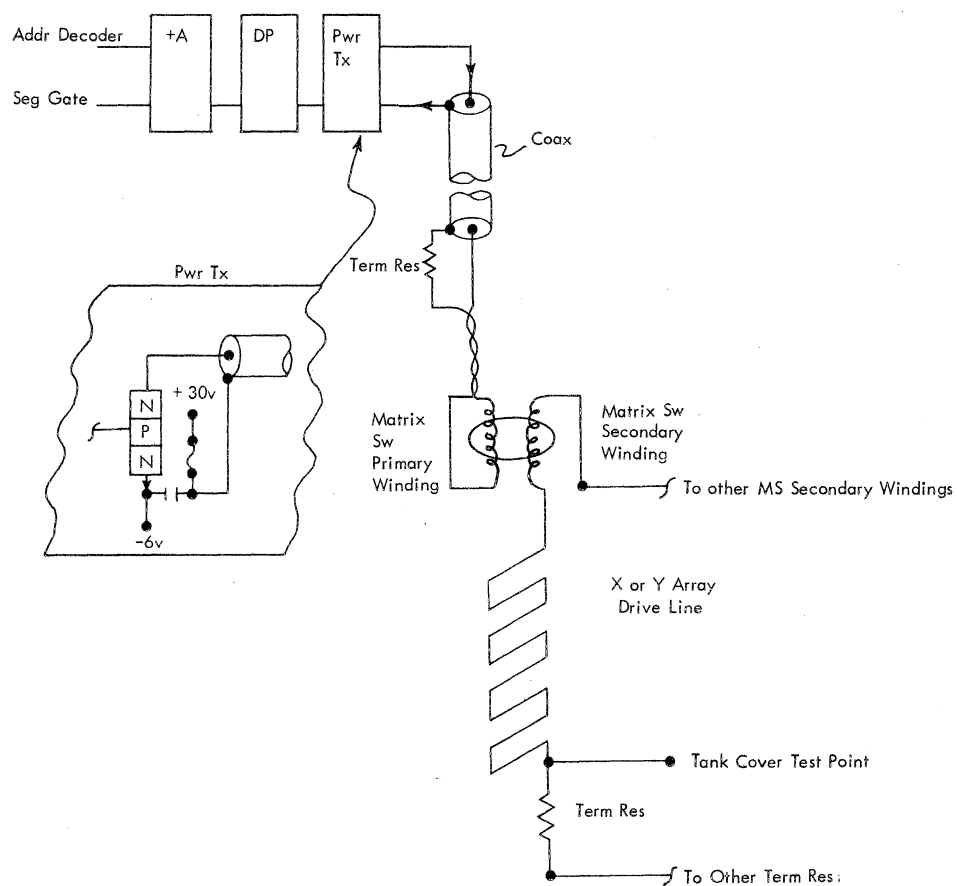
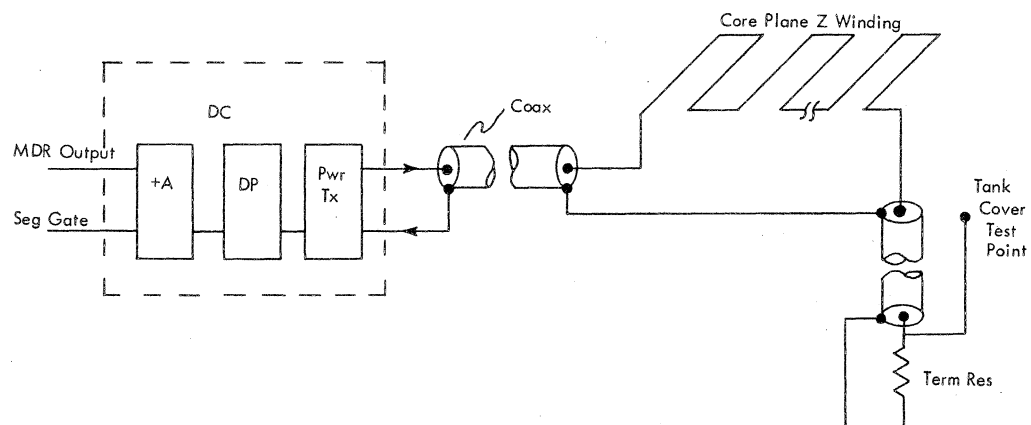


FIGURE 3.3-12. DRIVER FOR X, Y, AND Z DRIVE LINES

3.3.11 Timing Error Detection

A timing error is an indication that core storage was sent a second memory select pulse before the first core storage cycle was completed. Core storage circuits prevent the memory unit from recognizing any memory select that is received while it is in an operation cycle (Figures 3.3-13 and 14).

When a memory select pulse is received, the X, Y, Z, and Rd-Wr timing triggers are turned on. Outputs from the X, Y, or Z timing triggers turn on the error timing trigger which blocks the X, Y, Z, and Rd-Wr timing trigger input AND circuits until the end of the cycle. Thus, a second memory select pulse in less than 2 usec cannot initiate false timing pulses. Instead, the memory select pulse is gated out to the CPU through an AND circuit, indicating a timing error.

The timing error trigger initiates a reset for the timing triggers. When the first timing trigger turned on, it turned on the timing error trigger causing an up level at point A which feeds a single-shot circuit composed of Dly₁, C1, and A1. Output B is a negative pulse of fixed duration which is further delayed through Dly₂. Output C is the delayed pulse which resets all of the timing triggers. All of the timing triggers should be off before the timing error gate (pulse C) is received; however, the timing error gate is an additional reset and also resets the timing error trigger.

The timing error gate serves another purpose. Assume the Z timing trigger is turned on due to noise caused by a power off-on condition of another modular unit in the system. Since the Z timing trigger was turned on without a memory select, no normal reset is available to turn it off. The timing error trigger will provide a pulse (timing error gate) to reset the Z timing trigger and also to prevent a memory select from initiating a core storage cycle until all of the timing triggers are reset.

3.3.12 Customer Engineer Test Panel

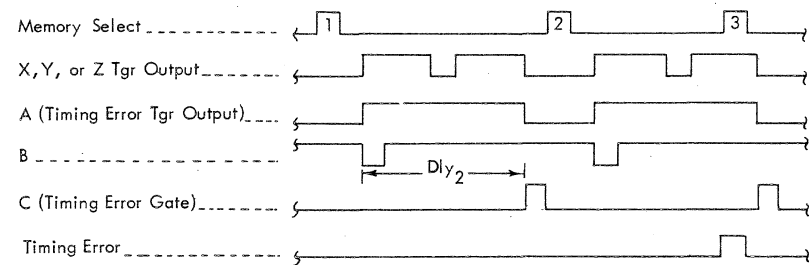
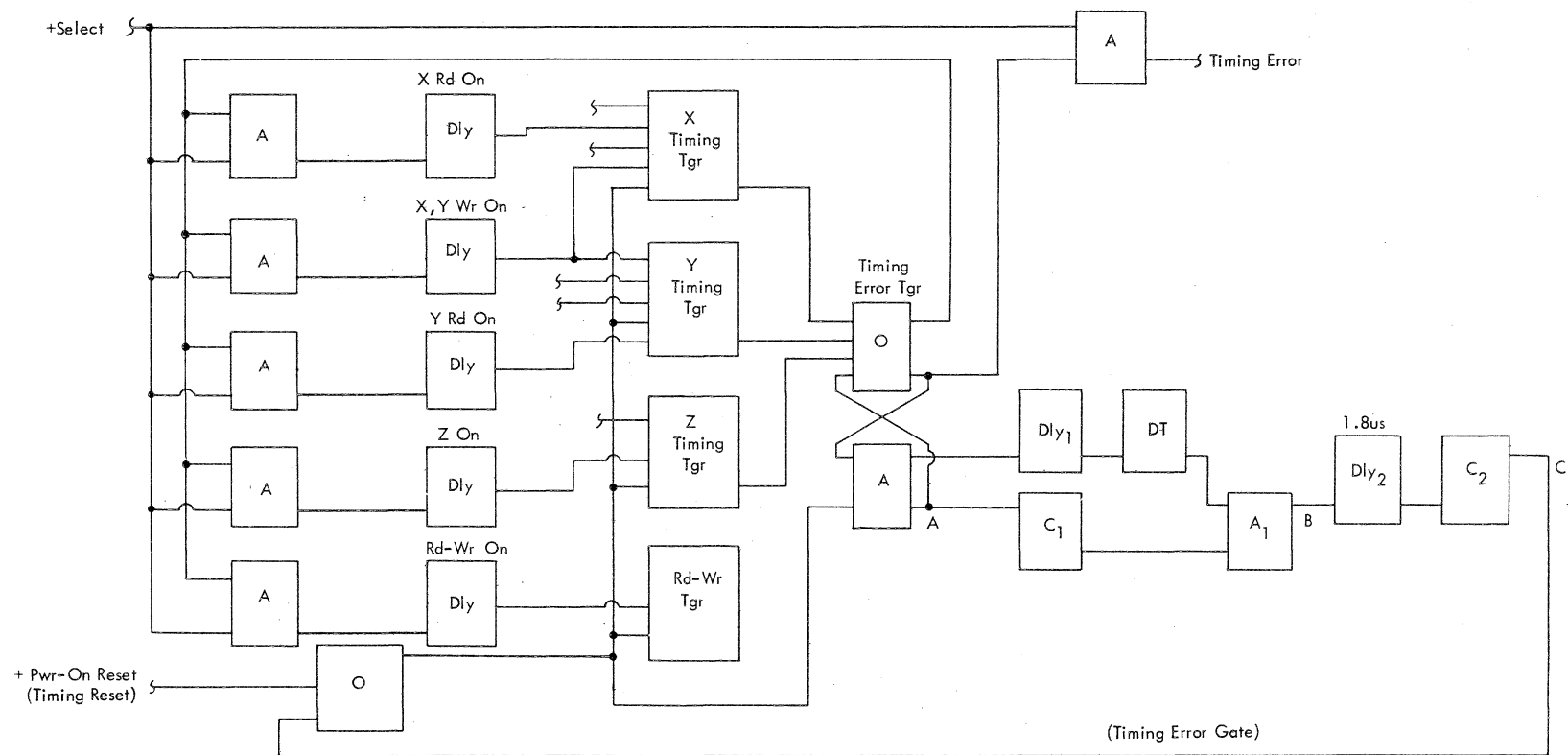
A core storage test panel is located in the core storage modular unit to assist in locating storage troubles. MAR and MDR indicator lamps are provided to indicate the position and address at which an error occurs (see Figure 3.3-15). An error-check trigger is used to signal the core storage unit when an error has occurred. When core storage is being tested the error-check trigger is reset on; an error condition will turn the trigger off. CE test panel circuits are shown in Figure 3.3-16.

Test On-Off Switch

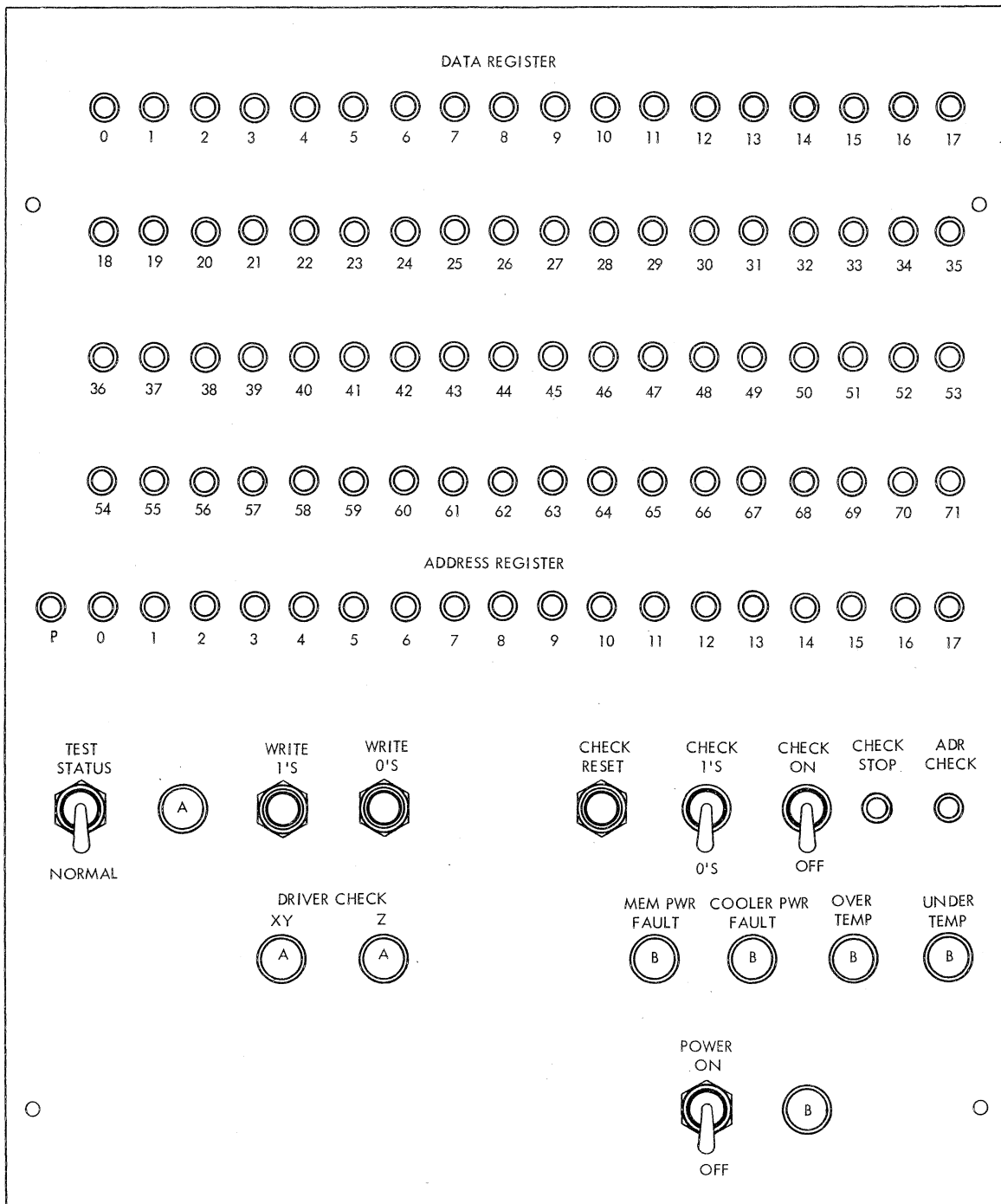
This switch, when off, holds the storage test error-check trigger off. When the switch is turned on, the error-check trigger is fed a short reset pulse to set the trigger on. The error-check trigger being on, signals the CPU to select core storage and proceed to step the MAR through all instructions. Thus, all addresses in storage are tested over and over.

Write-Ones Key

This key kills the Z timing gate. No inhibit current can flow and all addressed cores are set to a 1 status during the write portion of the core storage cycle (Figure 3.3-17). The write-ones key is inoperative when the error-check trigger is off. The write-ones key must be held down until ones are written in all addresses.

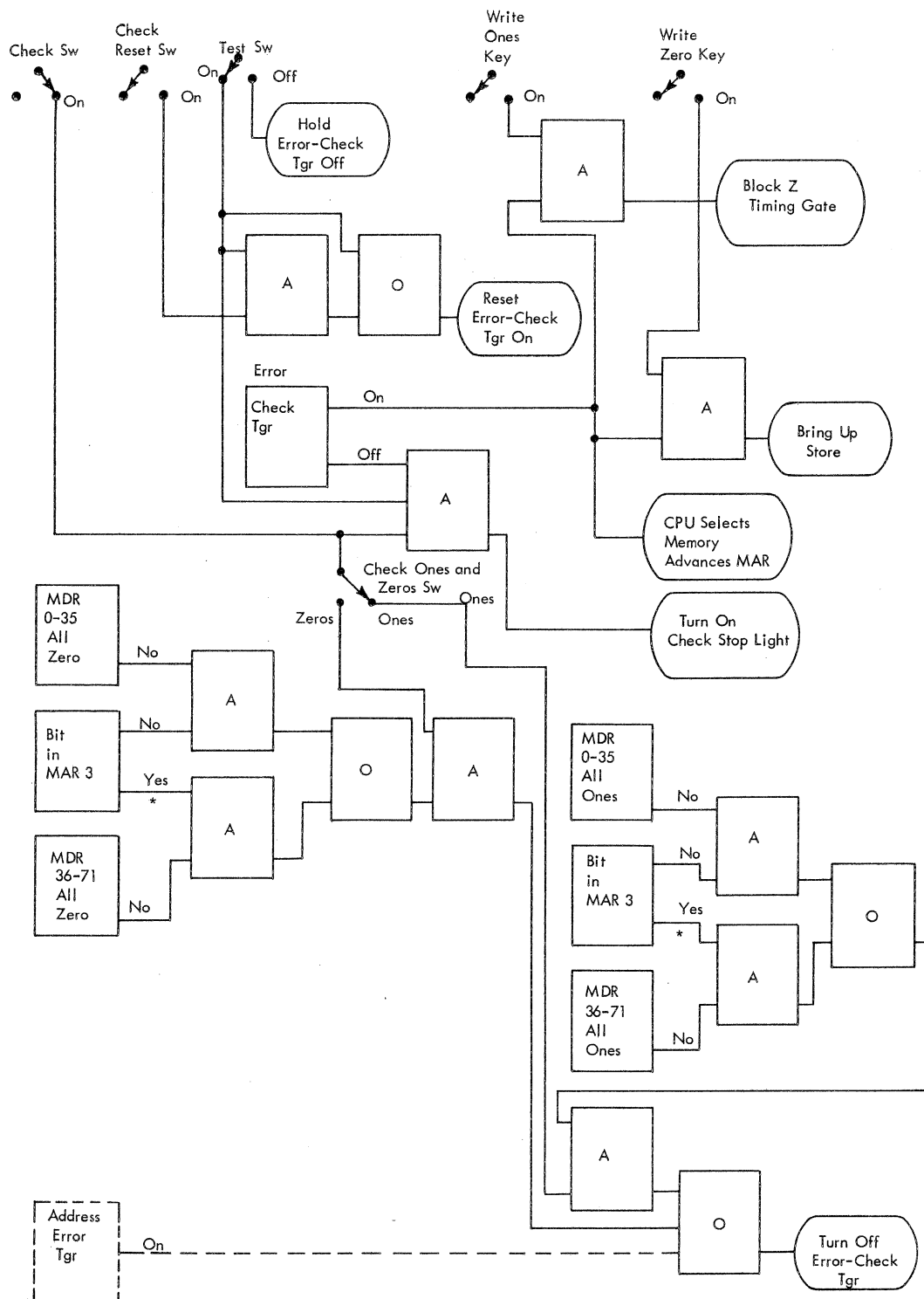


FIGURES 3.3-13 & 14. TIMING ERROR DETECTION & WAVE FORMS



A = 6v Lamp
B = 48v Lamp

FIGURE 3.3-15. CE TEST PANEL



* Both Outputs of MAR 3 Are Used on Not 7090 Systems

FIGURE 3.3-16. CE TEST PANEL CIRCUITS

Write-Zeros Key

This key brings up the store line and holds the read-out line down. The strobe pulse to the sense amplifier is killed, and the addressed cores are set to a 0 status (see Figure 3.3-17). The write-zeros key is inoperative when the error-check trigger is off. The write-zeros key must be held down until zeros are written at all addresses.

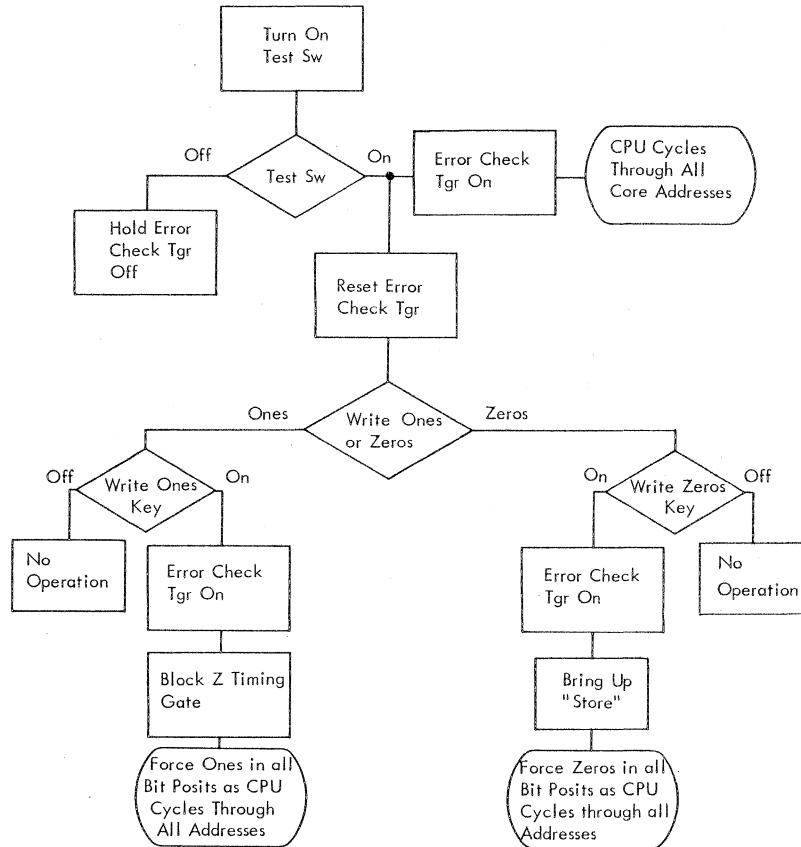


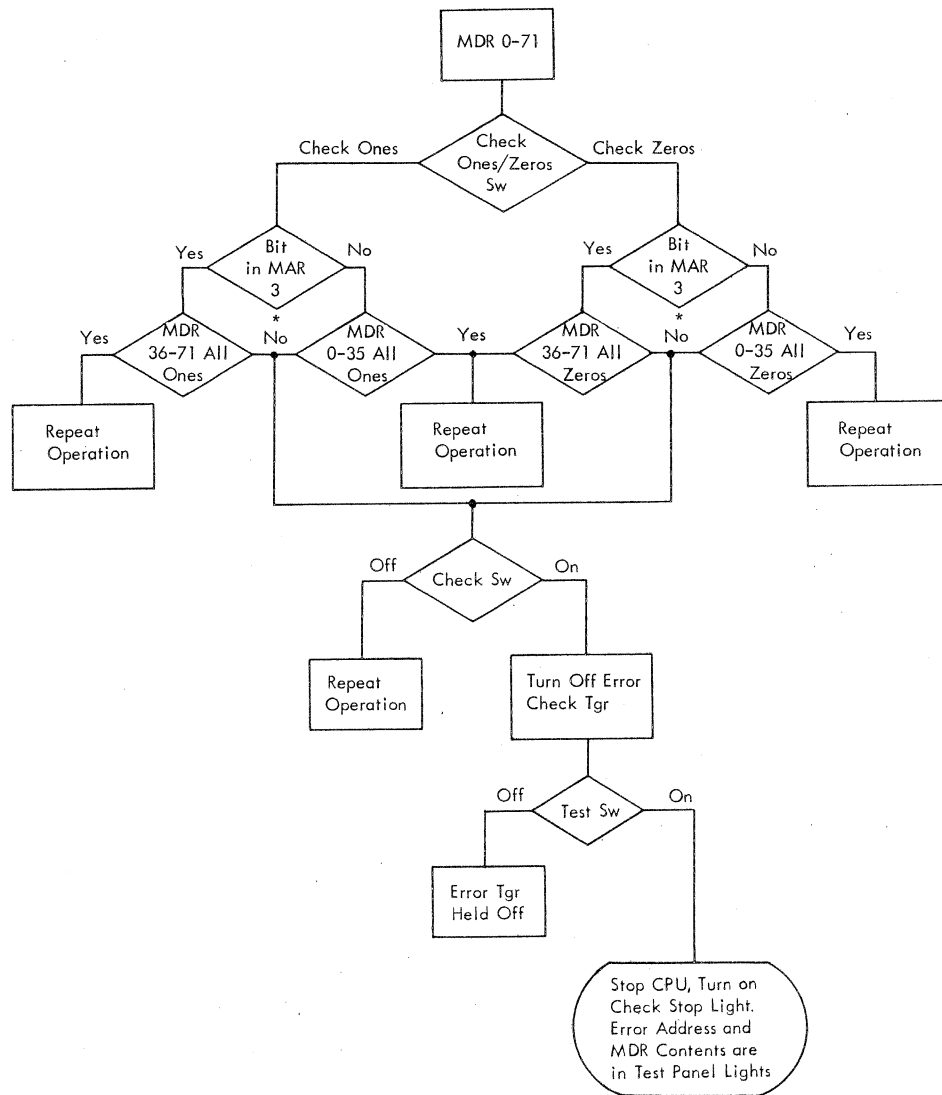
FIGURE 3.3-17. WRITE ONES OR ZEROS

Check Switch

Check switch when on allows an error to turn off the error-check trigger which, in turn, stops the CPU from cycling and turns on an error indicator. With the check switch off, an error condition cannot turn off the error-check trigger so the unit will continue to cycle through all addresses.

Check Ones-Zeros Switch

This switch, in conjunction with the check switch on, causes the error-check trigger to turn off if an error occurs (Figure 3.3-18). If ones are being tested, the ones-zeros switch must be in the test ones position. When testing zeros, the ones-zeros switch must be in the test zeros position.



*Both MAR 3 Outputs Are Used in Not 7090 Systems

FIGURE 3.3-18. TEST ONES OR ZEROS

Check-Reset Key

The check-reset key, when depressed, resets the error-check trigger on so the CPU will again cycle core storage through all addresses. However, if the storage unit is not reset to its original all ones or zeros status another error will be recognized when the original error address is reached. The normal procedure following an error is as follows:

1. Turn off check switch.
2. Depress check-reset key.
3. Depress either write-ones or write-zeros key to reset all core storage addresses.
4. Turn on check switch and continue with test.

Error Trigger Resets

The error-check trigger may be reset on with the check-reset key or by turning the test switch on. Both resets use a circuit similar to a single-shot which resets the trigger for only a short period of time; therefore, the test switch being on, or holding the check reset key down, does not hold the error-check trigger reset.

Customer Engineer Panel Indicators

Indicators to assist the customer engineer are:

Check stop -- An error is recognized while testing core storage.

Address check (not 7090) -- An address error is recognized.

XY Driver check -- A neon in the X or Y core driver circuits turned on.
In normal operation the neon will never ionize. Neon detection circuits and a description of their operation is included in the power supply manual.

Z Driver check -- A core driver neon in the inhibit circuits turned on.

Memory Power Fault -- Blown fuse in core storage power supply.

Cooler Power Fault -- Fault in core cooling unit, recognized by loss of oil pressure or oil is too hot.

Over Temperature -- Core cooling oil is 110° F or over; normal operating temperature is 104° F.

Under Temperature -- Core cooling oil is 98° F or below.

Power-On Indicator -- Lights when all DC voltages are up in core storage unit.

CE Test Light -- Indicates C. E. test switch is on.

Error Address Analysis

Analysis of the CE panel error address is an aid to isolating core storage troubles. From the error address, the Z segment, X segment, Y segment, and sense amplifier segment may be determined. Figure 3.3-19 gives the MAR positions required to determine all array segments. Swapping SMS cards within a register is the simplest method of analysis. All SMS cards may be swapped freely within a register.

X Segment: MAR 15, 16, and 17 Selected segment equal to octal value of MAR positions.
Y Segment: MAR 8, 9, and 10 Selected segment equal to octal value of MAR positions.
Z Segment: MAR 4 and 5 $Z_A = \text{MAR } 4, \text{ MAR } 5$ $Z_B = \text{MAR } 4, \overline{\text{MAR } 5}$ $Z_C = \overline{\text{MAR } 4}, \text{ MAR } 5$ $Z_D = \overline{\text{MAR } 4}, \overline{\text{MAR } 5}$
Sense Ampl Segment: MAR 11 and 12 $SA_A = \text{MAR } 11, \text{ MAR } 12$ $SA_B = \text{MAR } 11, \overline{\text{MAR } 12}$ $SA_C = \overline{\text{MAR } 11}, \text{ MAR } 12$ $SA_D = \overline{\text{MAR } 11}, \overline{\text{MAR } 12}$

FIGURE 3.3-19. SEGMENT DETERMINATION

Address circuitry failures require more analysis than register failures. However, it is seldom necessary to scope more than 32 lines to isolate the trouble. If the error address always appears in the same segment, either one or more of the core drivers within the segment is probably at fault or the segment circuit is failing.

Error addresses in any or all segments suggest a failure in the memory address driver lines. Recall that the 32 driver lines are composed of 16 complement pairs. Sixteen of the lines conduct during the read time and the other 16 during write time. By programming, a single core storage address may be read repeatedly while all 32 lines are scoped; each line should conduct during one half of each core cycle. It is possible to determine which lines should conduct, but all 32 lines can be scoped easier and quicker.

Scoping is necessary to locate open core driver transistors; shorted core driver transistors will light the neon on the back of the panel making them easy to spot.

3.3.13 Core Cooling

A core cooling unit is located in the lower right-rear section of the core storage modular frame. The cooling unit maintains the temperature of the oil in the array tank at $104^{\circ} \pm 2.5^{\circ} \text{F}$. The cooling unit can both heat and cool the oil. Oil heating is accomplished with three 1000 watt heating elements and oil cooling is done with a heat exchanger, which looks like a small radiator, and a fan.

Indicators

The following indicators are mounted on the core storage CE panel to assist the customer engineer:

Under temperature -- Tank oil temperature is $98^{\circ}\pm 1^{\circ}\text{F}$ or below.

Over temperature -- Tank oil temperature is $110^{\circ}\pm 1^{\circ}\text{F}$ or over.

Cooler power fault -- Drops power to the core storage unit; recognized by lack of oil pressure or excessive oil temperature. A cooler power fault also turns on a fault light on the console unit.

Electrical Circuits

Electrical circuits which control the operation of the core cooling unit are shown in Figure 3.3-20. Note that the oil cooling unit is energized when the wall switch is closed and is not dependent on power being brought up on the system. Energizing the oil pump motor builds up pressure, closing the pressure switch at 20 ± 3 psi which energizes the heater control relay. Assuming the wall switch was just closed; the warm-up thermoswitch is closed opening a valve which allows the oil to pass through the heater unit and directly back to the array tank.

The oil heater units are energized when the heater control relay is picked. The heater units are further controlled by thermal switches. Oil flows through the heaters and back to the tank until the temperature of the oil reaches $95^{\circ}\pm 1^{\circ}\text{F}$. Then the warm-up thermoswitch opens. Opening the thermoswitch closes the by-pass valve and a mixing valve now controls the oil temperature. The mixing valve mixes oil from both the heater unit and the heat exchanger in a proportion that maintains an output oil temperature of $104^{\circ}\pm 2.5^{\circ}\text{F}$. The heaters continue to heat the oil until the thermoswitches (in series with the heaters) open at $109^{\circ}\pm 1^{\circ}\text{F}$.

All thermals are of bi-metal construction; as the temperature varies, the thermal unit actuates a plunger which in turn operates a microswitch.

A heater interlock thermoswitch in series with the pressure switch is an overheat protection device which drops the heater control relay if the oil temperature exceeds $115^{\circ}\pm 1^{\circ}\text{F}$. One set of normally open heater control relay points is in the core storage power-on interlock circuits; therefore, the heater control relay must be energized to bring power up on the core storage unit. If the relay is dropped, the same interlock point drops power to the core storage unit.

Oil Flow

Oil flow and thermal unit locations are shown in Figure 3.3-21. Note that all thermals are located within the cooling unit rather than in the array tank. Physical location of the thermals and valves are shown in Figure 3.3-22.

The core cooling system uses 42 gallons of transformer oil. Minimum rate of flow is 5.7 gallons per minute, and maximum oil pressure should not exceed 80 psi.

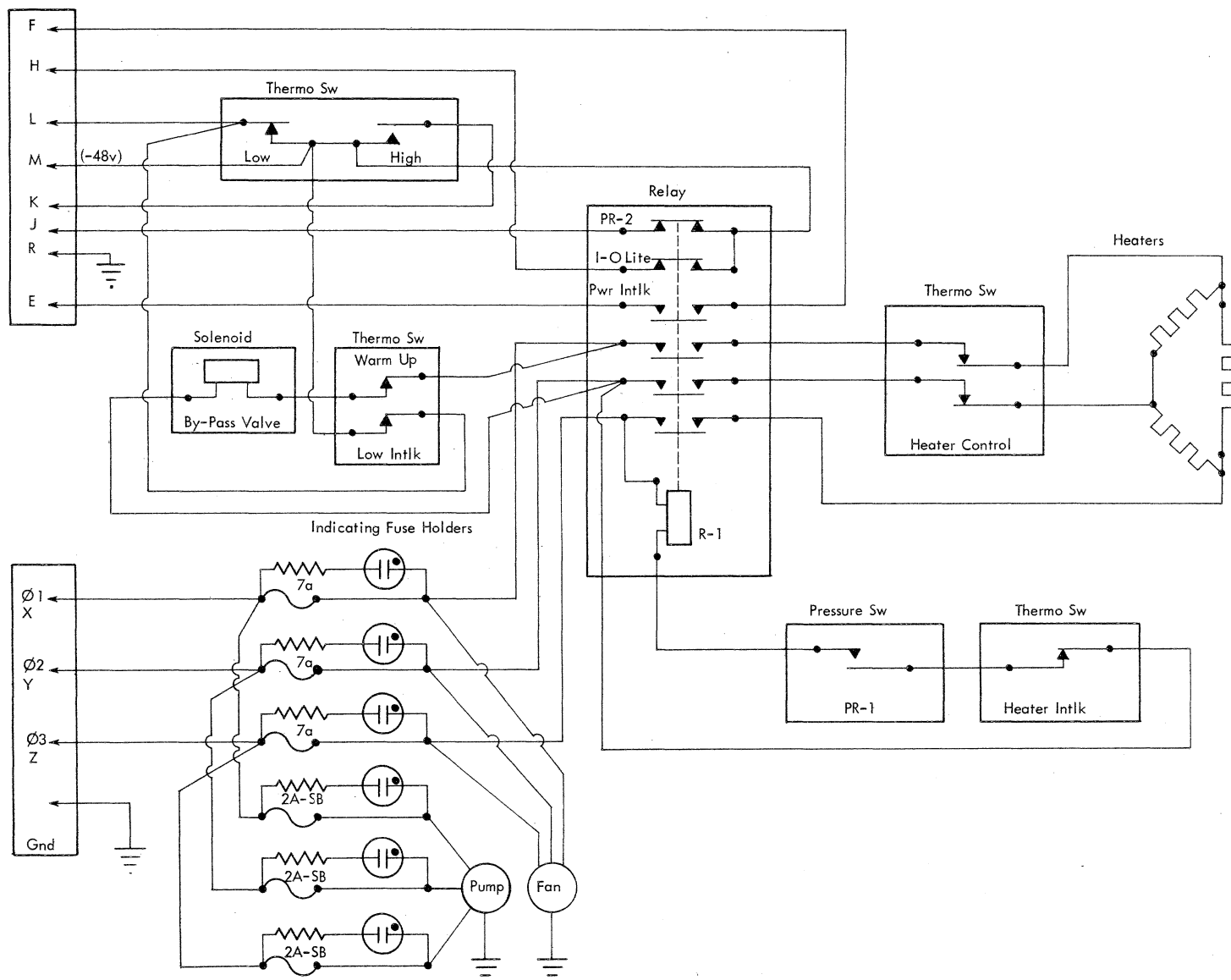


FIGURE 3.3-20. CORE COOLING CIRCUITS

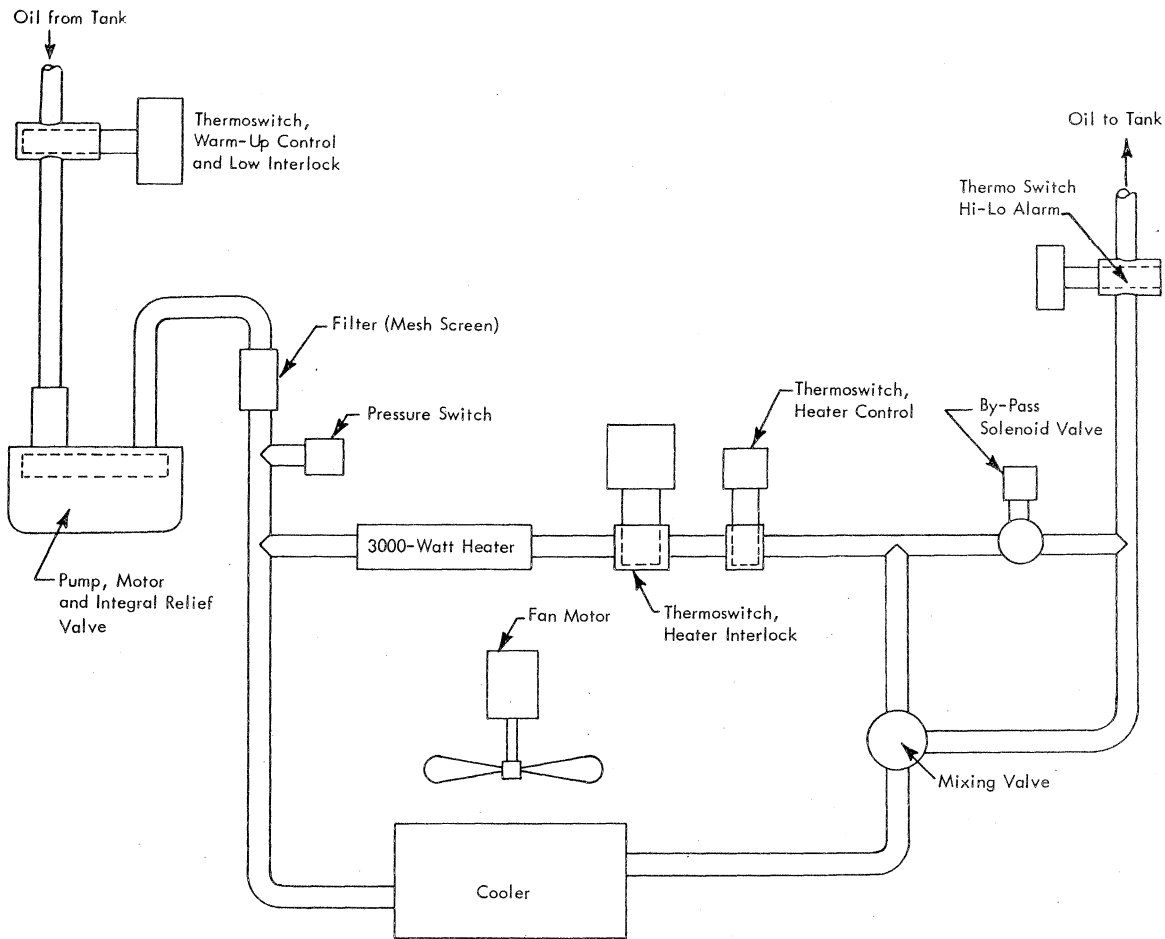


FIGURE 3.3-21. CORE COOLING OIL FLOW

CAUTION

The transformer oil used in the core cooling unit is classified as combustible. The oil is relatively non-hazardous; it is not particularly toxic and has a high flash and fire point. However, if the oil is atomized or is in a thin film, a match will ignite it easily. The Safety Department warns that the oil, improperly used, could be a hazard. As a result, the following rules should be observed:

1. NO SMOKING should be allowed in the area where oil is put into and taken out of the array tank, or around the array when it is removed from the oil.
2. Protect wood floors to keep them from absorbing oil.
3. Before soldering an array, allow it to drip long enough to remove excess oil.
4. Do not solder over the tank without draining the oil. This would not cause a fire hazard but solder drops could cause shorts during machine operation.
5. Oil leaks which atomize the oil can be dangerous since a spark or flame can ignite the oil.
6. Keep oil soaked rags in closed metal containers with proper identification.
7. Wear protective clothing when working around any portion of the unit where oil is found.

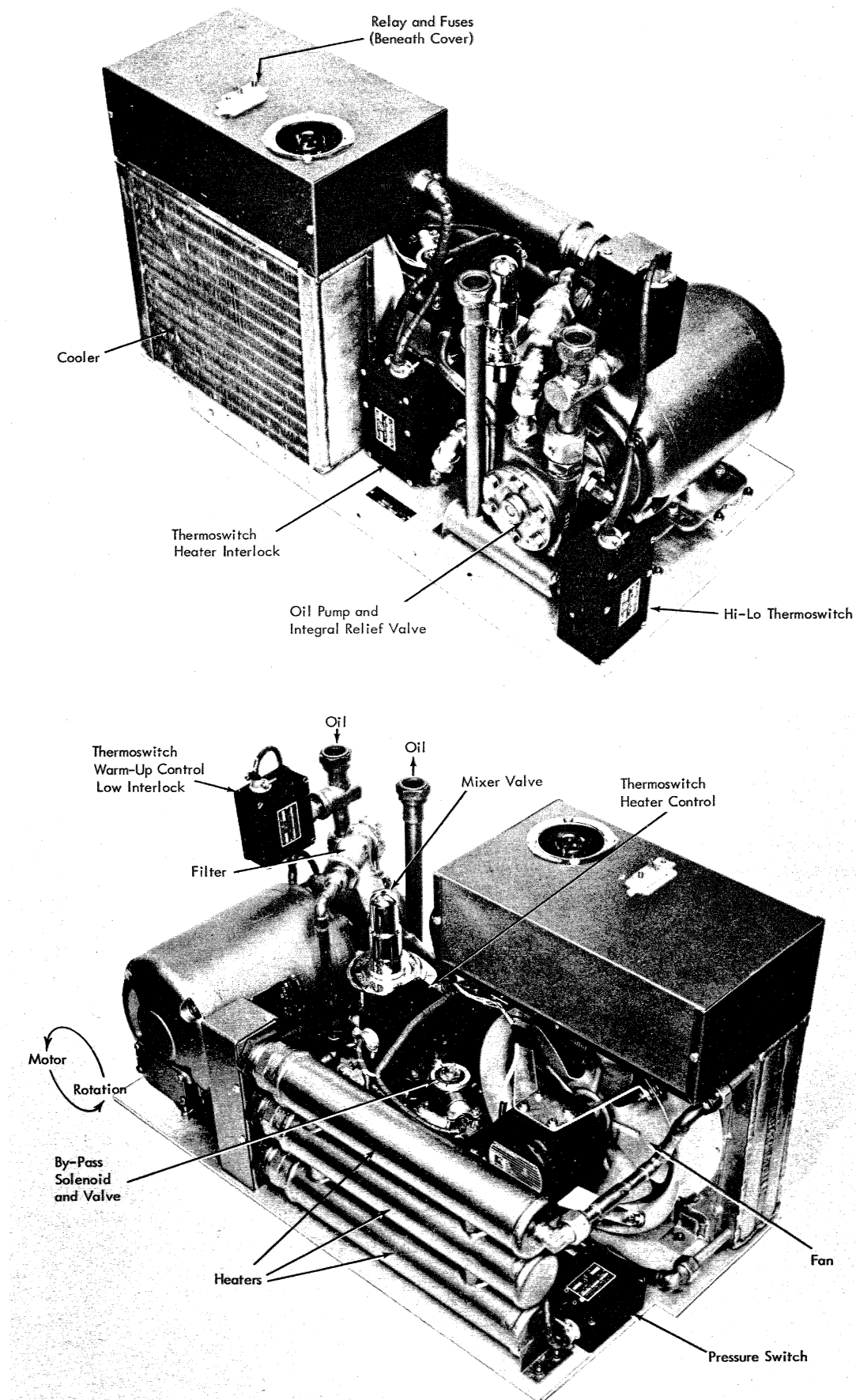


FIGURE 3.3-22. CORE COOLING UNIT

4.0.00 SPECIAL CIRCUITS

4.1.00 Memory Address Register

The memory address register (MAR) is a latch type register which will hold a "one" status until impulsed with a "zero". The "zero" status will then hold until a "one" is again read in.

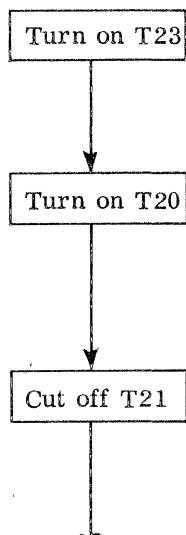
Figure 4.1-1 is a schematic diagram of a MAR position. Physically, two MAR positions are located on one double card.

As an aid in following the circuit, all transistors in conduction when the circuit is in a "one" status are drawn with a solid outline; transistors which conduct for a "zero" status are drawn with a dotted line; transistors which conduct for either status are drawn with a double outline. Transistors T23 and T25 are drawn with a double outline and labeled because they are part of the input AND circuit and conduct to set the circuit to a particular status but are cut-off when memory select falls.

Assume a "one" is to be read into the MAR which is initially in a "zero" status (T16, T17, T21 conducting). Transistor T24 is a supervisory input; therefore, when memory select is down at a $-2v$, transistor T23 or T25 cannot be forward biased.

When a memory select pulse is received and there is a bit on the MAR line, T23 will conduct; circuit operation is:

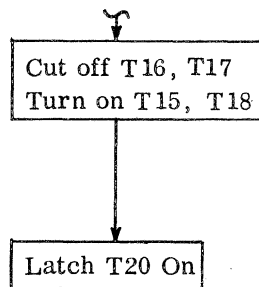
Set MAR to A One Status



Memory select is up, MAR line is down. The output of T23 was initially $-6.8v$; while in conduction, its level is clamped at $-5.4v$ by the clamp circuit of T14.

T25 is cut off; therefore, the base lead of T21 is at $-6.0v$. Point A at the emitter common of T20 & T21 is about $-6.0v$ so the $-5.4v$ input to T20 forward biases it into condition.

With $-5.4v$ at the base of T20, point A of T20 and T21 emitter commons are about $-5.4v$. Because base of T21 is at $-6.0v$ it is reverse biased and cut off.

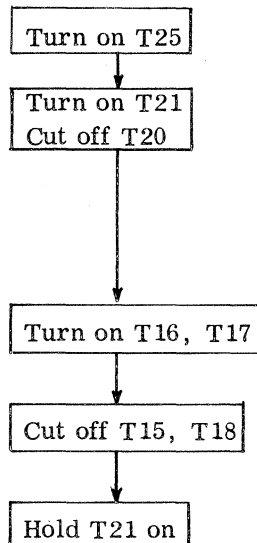


When T21 is cut off, its collector output voltage rises to +0.4v, reducing the current through T16 and T17 and allowing T15 and T18 to go into conduction. T15 and T18 will hold T16 and T17 cut off.

T15 conducts through the collector circuit of T23 to maintain a -5.4v level to T20 which continues to hold the condition even after memory select falls and T23 is cut off.

Set MAR to A Zero Status

When a zero is read, memory select comes up but, because there is no bit on the MAR line, the MAR line will also be up. Circuit operation is:



Memory select and the MAR line are both up.

When T25 goes into conduction, its output rises from -6v to -4.3v; because point A in the emitter circuit of T20 and T21 is at -5.4v, transistor T21 is forward biased. Then T21 goes into conduction, point A goes to -4.3 v, and T20 is cut off.

Output of T21 falls from +0.4v to -2.0v which forward biases both T16, T17.

T16 and T17 going into conduction reverse biases both T15 and T18.

When memory select falls, T25 is cut off. However, the output of T25 is -6.0v while the output of T23 is -6.8v. Thus T21 will remain forward biased and T20 is reverse biased.

Clamp circuits (T14 and T22) are used to prevent saturation of T23, T20, T21 and T15. If the transistors were allowed to saturate, the response time of the circuit would increase. Approximate forward resistance values of the clamp diodes are given in Figure 4.1-1.

4.2.00 SENSE AMPLIFIER

The sense amplifier circuit amplifies the signal from the four sense windings of each core plane. One sense amplifier is required for each of the 72 planes in the array.

Each sense amplifier has 4 class A differential amplifiers, one for each sense segment in a core plane. The four differential amplifier outputs are OR'ed together through an emitter follower (Figure 4.2-1) which, in turn, feeds a strobe gated amplifier. The output of the strobe gated amplifier is gated by a strobe pulse; therefore, an output from the sense amplifier is available only while a strobe pulse is present. A level setter on the output of the sense amplifier is used to obtain a P level output.

Figure 4.2-1 shows a sense amplifier circuit with one differential amplifier. Transistors T1 and T2 form the differential class A amplifier. The input signal to the amplifier may be either a positive or negative pulse of approximately 130 mv. The DC level of the input voltage may vary but its affect will be cancelled in the primary of transformer T₁. Resistors R₁ and R₂ are feedback resistors which desensitize the circuit to prevent ringing and make the choice of components non-selective. Capacitor C₁ is used to improve circuit response time.

Assume an input signal with point A going positive. Conduction through transistor T1 increases and through T2 decreases as point A goes more positive. The change of flux in the primary winding of transformer T₁ is equivalent to the total change of current through both Transistors T1 and T2. Transformer T₁ is an isolating pulse transformer with a one-to-one turns ratio.

Noise from all sources is amplified by the differential amplifiers from each segment and fed through the emitter follower. To prevent large noise pulses from causing erroneous outputs, the input of the strobe gated amplifier is clamped with diode D₁. Diode D₁ clamps all noise and input pulses at approximately +1.0v. Transistor T23 is held cut-off until a strobe pulse is received because the base is clamped so it can never go more positive than +1.0v and the emitter is held at +2.0v. A strobe pulse attempts to bring the emitter of T23 to -1v; however, diode D₂ will clamp the emitter at ground level. Because the voltage on the base of T23 can vary from -0.4v to +1.0v the transistor can be forward biased to produce an output for the duration of the strobe pulse.

4.3.00 MEMORY DATA REGISTER

The memory data register (MDR) is basically a trigger with an input and an output AND circuit. The input AND circuit has a supervisory input; the trigger and the output AND circuit are both standard circuits with standard voltages.

Figure 4.3-1 is a schematic diagram of a MDR. Two MDR positions are mounted on one double card.

The signal level (supervisory input) of the data-in-gate is -2.0v or +0.4v. When the data-in-gate is at -2.0v, the emitter common of T24 and T25 will also approach -2v. As a result, T24 cannot be forward biased because the base lead of T24 has signal levels of +0.4v or -0.4v.

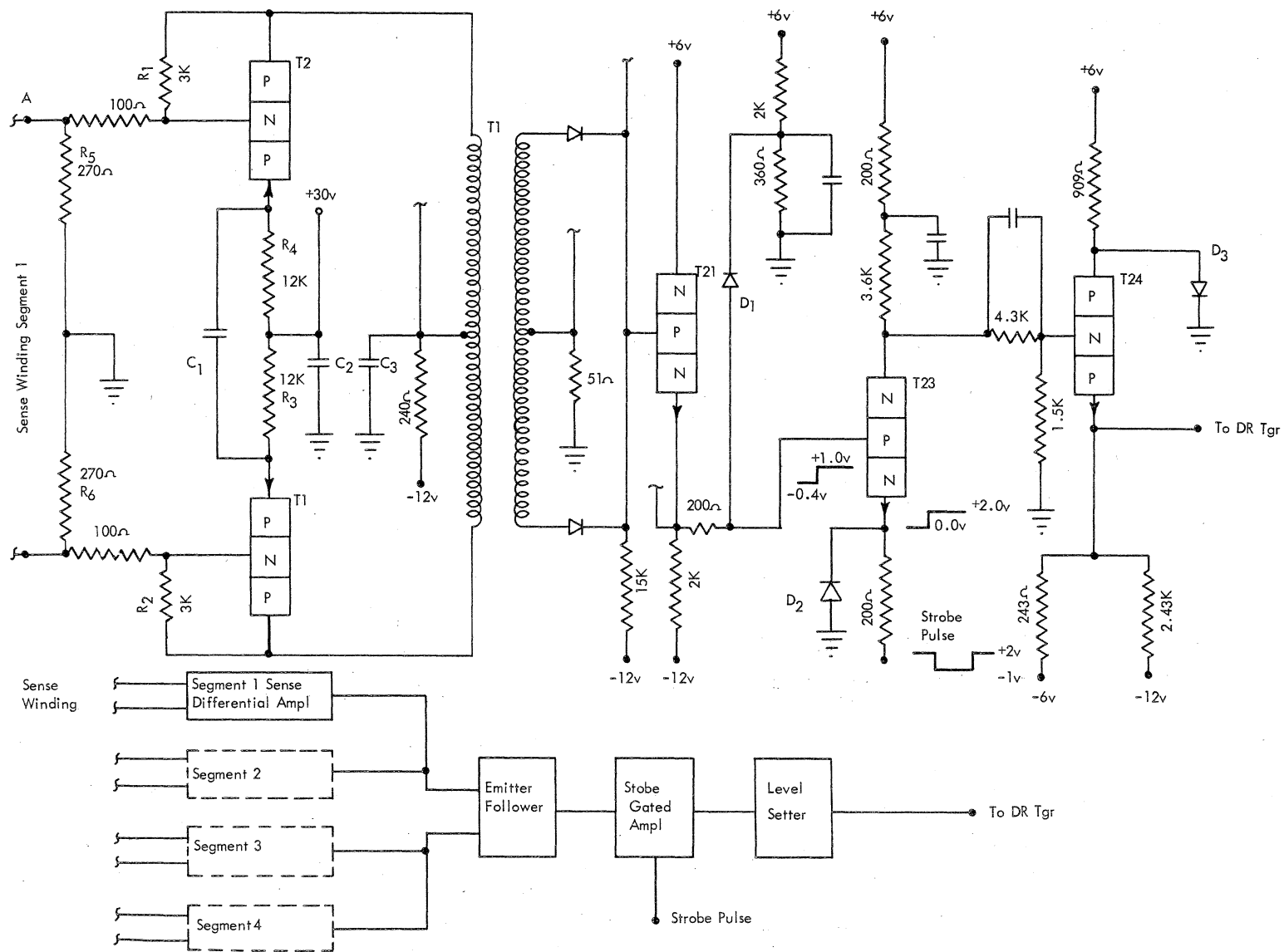


FIGURE 4.2-1 SENSE AMPLIFIER

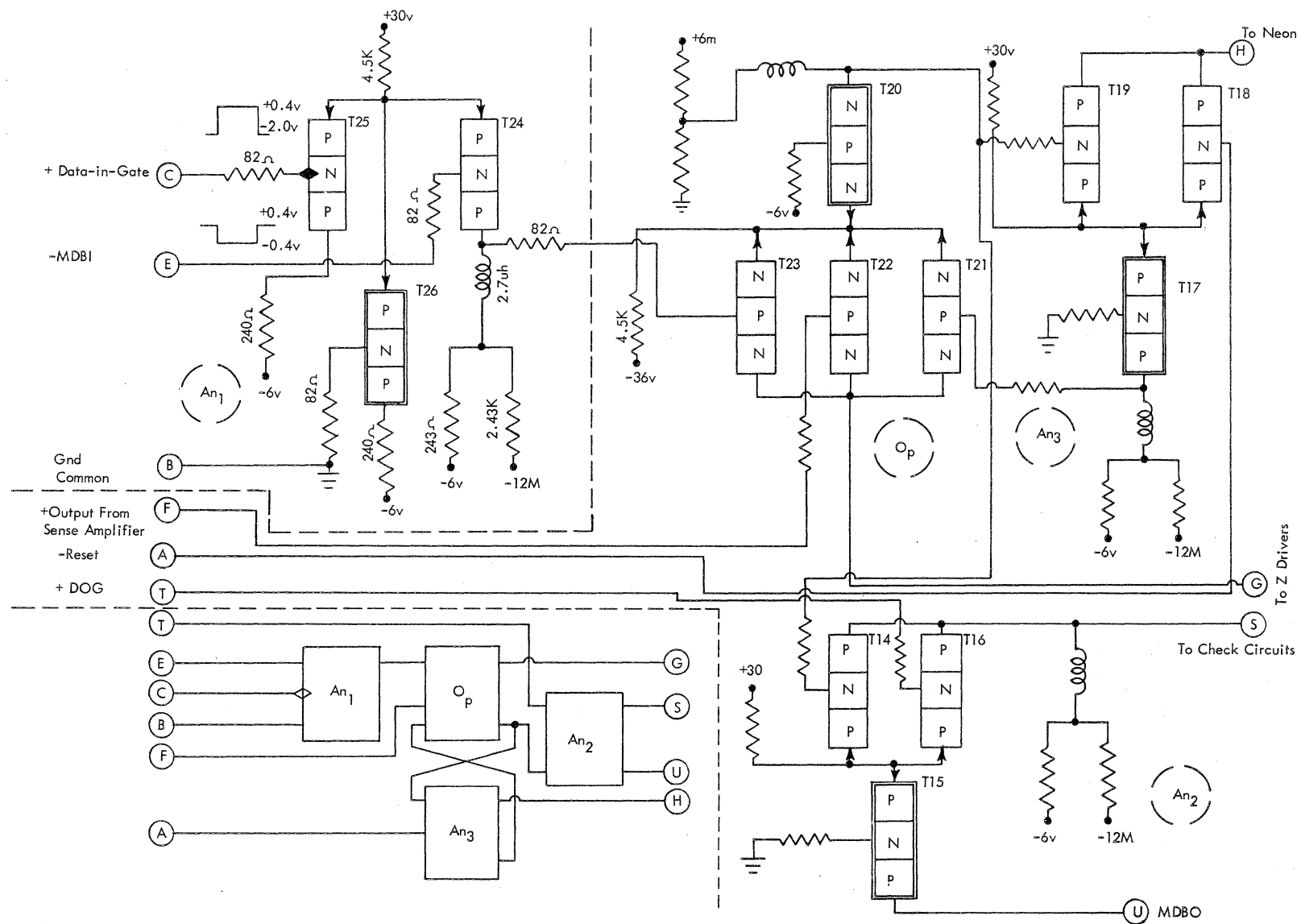
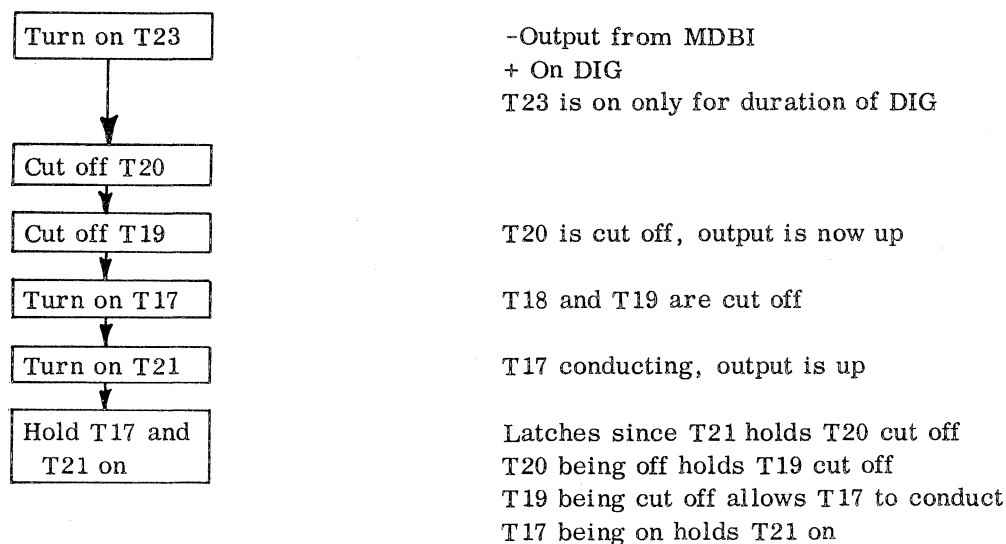


FIGURE 4.3-1. MEMORY DATA REGISTER

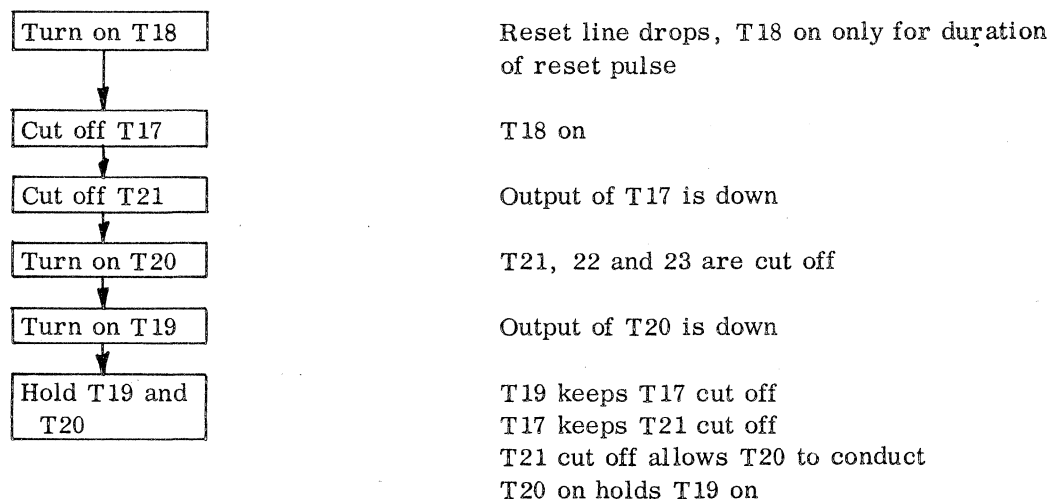
When the data-in-gate is up and the memory-data-bus-in line is down, transistor T24 conducts, feeding a positive pulse to T23 which turns the trigger on. An output pulse from the sense amplifiers does not go through the input AND circuit; instead it feeds directly into the trigger, turning on T22.

Sequence of operations to turn the trigger on with a bit from the MDBI is:



To turn trigger on with an output from the sense amplifier, substitute T22 for T23 in the first block; the rest of the circuit is identical.

Sequence of operations to Reset MDR:



Two outputs are available from the MDR. The two outputs are to Z drivers and to memory data bus out (MDBO). Output to Z drivers feeds directly from the trigger; output to MDBO is gated through an AND circuit (T14 and T16) with a data-out-gate.

4.4.00 CORE DRIVER

A core driver (DC) is basically an AND circuit feeding a power driver which drives a power transistor. Core driver circuits for both X-Y drivers and Z drivers are schematically identical (Figure 4.4-1), but each circuit uses different power transistors and collector voltage (X & Y drivers use a type 93 power transistor and 30v collector voltage; Z drivers use a type 89 power transistor and 60v collector voltage.).

Assume input E is at an up level and input F is down: T8 will be conducting and the output of T6 will be -9v. If the segment gate (input F) now goes positive, T8 cuts off and T6 conducts, causing output to rise to -4.0v. Transistors T4 and T5 power the output of the AND circuit to drive the power transistor.

The output of the power transistor will be +60v or +30v initially. When the transistor goes into conduction the collector voltage attempts to drop to -6v. A 3v zener diode in conjunction with an Fs diode and a resistance to -36v, forms an inverse feedback circuit which feeds back part of the output signal to T6 which, in turn, clamps the power transistor output at -3v. Point A in the feedback circuit varies from +57v or +27v to -6v. However, when point A becomes more negative than -4v, diode Fs is forward biased and feeds current to T6. Transistors T4 and T5 reflect the T6 output to the power transistor to reduce its forward bias. The result is that the output of T6 stabilizes at -6v, and the power transistor output stabilizes at -3v.

The purpose of the feedback circuit is to prevent the power transistor from going into saturation. If the power transistor goes into saturation, its cut-off time will increase appreciably, causing faulty operation particularly during the transition from read cycle to write cycle time for X or Y drive lines and as noise on sense lines for Z drivers.

The resistance in the feedback circuit is the total of 6 individual resistors. Individual resistors are used to allow even distribution of heat, eliminating hot spots.

The -6v source used in the DC circuit is the regulated supply located in the core storage special voltage power supply. Realize that there are 800 core drivers; as a result, the load on the -6v supply can vary over a wide range and considerable noise will be introduced. To compensate for the noise on the -6v line, de-coupling capacitors are used in the collector circuits of T4 and T5. The effect of the capacitors is to allow the circuit to ride, or float, with the noise, thus preventing the noise from changing the characteristics of the circuit.

The neon in the collector circuit of the power transistor is a trouble shooting aid; if a power transistor shorts out, the neon glows indicating the unit in error. During normal operation the neons do not glow. The neons are on the back panel behind the core driver card.

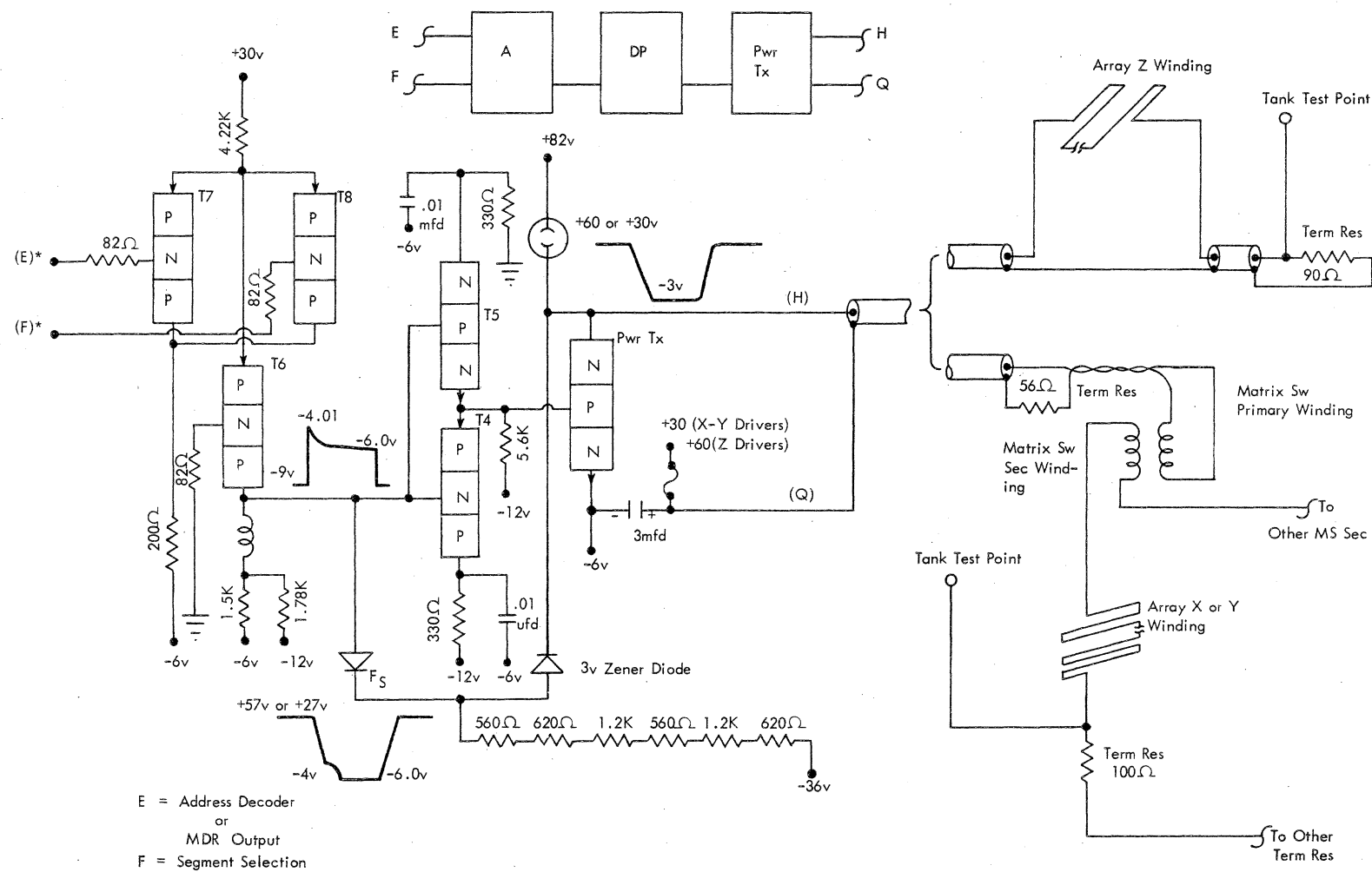


FIGURE 4.4-1. CORE DRIVER AND ARRAY WINDINGS